DESIGN AND DEMONSTRATION OF HIGH-PERFORMANCE ULTRA-THIN ANTENNA-INTEGRATED 3D GLASS-BASED MM-WAVE PACKAGES

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DESIGN AND DEMONSTRATION OF HIGH-PERFORMANCE ULTRA-THIN ANTENNA-INTEGRATED 3D GLASS-BASED MM-WAVE PACKAGES

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Dreaming, Designing, and Getting it Done!

Georgia Tech ECE

To my family and friends

ACKNOWLEDGEMENTS

When I came to the Georgia Tech Packaging Research Center in August 2015, it was my first time in the U.S. From the beginning of my stay, I was simultaneously confronted by the challenging research environment and the novelty of American culture. I have seen and learnt countless things, whether they were directly or indirectly related to research. I would like to thank all my friends and the people I have worked with, without whom I could not have accomplished my Ph.D.

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LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviations

3D	Three-dimensional
4G	Forth generation
5G	Fifth generation
ADS	Advanced design system
AiP	Antenna-in-package
BGA	Ball grid array
BiCMOS	Bipolar complementary metal-oxide-semiconductor
BPF	Band-pass filter
BS	Base station
CB-CPW	Conductor-backed coplanar waveguide
CCL	Copper clad laminate
CTE	Coefficient of thermal expansion
CMOS	Complementary metal–oxide–semiconductor
CMP	Chemical mechanical polishing
CO_2	Carbon dioxide

CPW	Coplanar waveguide
Cu	Copper
Df	Dissipation factor
Dk	Dielectric constant
EIRP	Effective isotropically radiated power
EM	Electromagnetic
eMBB	Enhanced mobile broadband
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
ENIG	Electroless nickel immersion gold
eWLB	Embedded wafer-level ball grid array
FBW	Fractinal bandwidth
FC	Flip-chip
FEM	Front-end module
FOWLP	Fan-out wafer-level packaging
GCPW	Grounded coplanar waveguide
GPE	Glass-panel embedding
HD	High-definition
HFSS	High frequency structural simulator
IC	Integrated circuit
IF	Intermediate frequency

IL	Insertion loss
IoT	Internet-of-Things
IPAC	Integrated passive and active component
IPD	Integrated passive device
LCP	Liquid crystal polymer
LNA	Low-noise amplifier
LPF	Low-pass filter
L/S	Line and space
LTCC	Low-temperature cofired ceramics
LTE	Long-term evolution
MCM	Multi-chip module
MIMO	Multiple-input-multiple-output
MMIC	Monolithic microwave integrated circuit
mMTC	Massive machine type communications
MS	Microstrip
NR	New radio
Q	Quality
QAM	Quadrature amplitude modulation
RDL	Redistribution layer
PA	Power amplifier
PCB	Printed circuit board

RF	Radio frequency
RL	Return loss
SAP	Semi-additive patterning
SiGe	Silicon Germanium
SIW	Substrate integrated waveguide
SMD	Surface-mounted device
SMT	Surface mount technology
SOC	System-on-chip
SOP	System-on-package
TGV	Through-glass via
TPV	Through-package via
TRL	Through-Reflect-Line
URLLC	Ultra reliable low latency communications
UV	Ultraviolet
VNA	Vector network analyzer

Symbols

f	Frequency
f_{c}	Center frequency / Cut-off frequency
$\tan\delta$	Dissipation factor
ϕ	Diameter / Azimuth angle

θ	Zenith angle
λ	Wavelength

SUMMARY

The fast-growing 5G wireless communications are emerging to transform a range of consumer and industrial sectors. Unlike 3G and 4G, mobile services are not the only market for the technology; fixed wireless access will also be a key use in 5G deployments. Fixed wireless access in sub-6 GHz can be used quickly with lower cost as the alternative to wired broadband. More importantly, millimeter wave 5G can perform a level of service bandwidth capacity that is comparable to fiber optics. 5G mm-wave systems require highly-integrated radio access solutions that incorporate advanced phased-array and antenna front-end technologies. Package integration of mm-wave components with antenna-in-package, therefore, is one of the key enablers for high-speed wireless applications.

The objective of the research is to model, design, and demonstrate high-performance ultra-thin antenna-integrated 3D glass-based mm-wave packages. Glass-based 5G mm-wave antenna module integration is presented here to achieve superior performance with miniaturization and manufacturability over conventional substrate technologies. The package-level integration for mm-wave elements and components into glass substrates offer higher component density, lower component-to-component signal losses, smaller footprint, thickness reduction, and equal to or lower cost compared to conventional organic- or ceramic-based substrates.

This dissertation presents electrical modeling and design, process development, fabrication, characterization, and analysis of high-performance ultra-thin antenna-integrated glass-based mm-wave packages with through glass vias. The first part of the dissertation focuses on high-density and low-loss package-level interconnects between components. The high-density low-loss interconnects include transmission lines in glass-core and re-distribution layers above the glass core, which provide 0.1 dB/mm at 28 GHz. In addition, this study in the glass-based substrate-integrated waveguides and with low-loss glass led to 0.018 dB/mm at 28 GHz. For high-density signal routing, impedance-controlled

sub-25-μm microvias with conformal shield are designed and precisely fabricated. 20-μm microvias resulted in a 10% reduction in insertion losses compared to 35-μm microvias.

The second part of this thesis describes the design and demonstration of heterogeneously-integrated *chip-last* mm-wave packages with seamless low-loss antenna-to-receiver signal transitions enabled by flip-chip assembly on panel-scale 100-μm thin glass substrates in the 28 GHz band. Building-block characterization results highlight the low interconnect signal losses as low as 0.021 dB/TPV at 28 GHz enabled by through-package vias. The Yagi-Uda antenna fabricated on glass substrates showed a center frequency of 25.85 GHz with a fractional bandwidth of 28.2%, which covers the 28GHz 5G frequency bands of interest. The antenna also featured a wide-angle main lobe at the target frequency range, implying good coverage of signal transmission and reception. This dissertation also discusses *chip-first* or chip-embedded mm-wave antenna-integrated modules that were demonstrated for the first time with panel-scale 100-μm thin glass substrates in the n257 band (26.5 – 29.5 GHz). New process advances were performed to reduce chip-to-package losses enabled by the chip-fist assembly into the glass substrates, which led to lower signal loss than the traditional flip-chip technology. Along with the details of the antenna design, feed-line modeling, and filter integration, glass-based MMIC-embedded antenna-integrated packages are validated and bench-marked against existing 5G substrate technologies such as organic laminate substrates and fan-out wafer level packages.

CHAPTER 1

INTRODUCTION AND BACKGROUND

Millimeter-wave (mm-wave) telecommunications for fifth-generation (5G) networks are emerging as a huge global market. 5G will impact our lives more dramatically than any technology shift since the internet itself simply because 5G leads to a fully connected world. The evolution of 5G communication systems has generated unique opportunities. Unlike 4G, which was limited to mobile phones, 5G is expected to be used in pervasive applications, and is expected to account for more than $400B, worldwide within the next decade, as shown in various trade reports. These applications are classified into three categories (Fig. 1.1): a) enhanced mobile broadband with multi-Gbps data rates (eMBB), b) ultra-reliable and low -latency ($<$ 1 millisecond) communications (URLLC) for mission-critical services such as high-definition (HD) and ultra-HD video streaming, known as 4K , and c) massive machine-type communications (mMTC) for autonomous driving, smart-cities, wearables, and smart-homes [1].

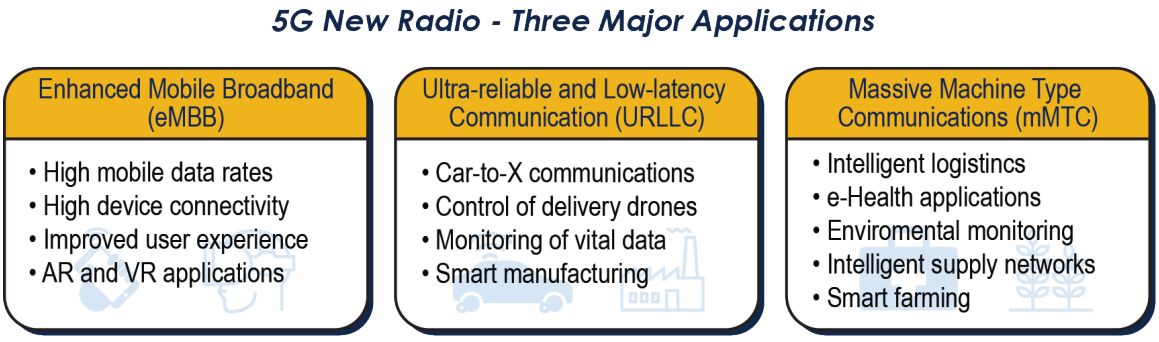

Figure 1.1: Major classes of applications with 5G networks.

Packaging of 5G systems needs integration of RF, analog and digital functions which includes both active and passive system components in a single module. These systems exemplify the heterogeneous integration trend. This becomes more important for 5G because of several reasons: a) integration of antennas with transceiver ICs and associated passive

and RF power divider networks, b) addition of sub-6 GHz (FR1) in the short-term with advances in packaging technologies, c) new mm-wave bands (FR2) drive the integration of new filters and diplexers along with broadband power amplifiers and switches, d) the add-on modules to the existing RFFE put additional emphasis on miniaturization and component integration. Proximity of the transceiver and front-end module is also important to reduce the size and losses. This is achieved by integration of antennas within the RF module as well as simultaneous heat dissipation solutions to keep active components in acceptable thermal conditions. Integration of power amplifiers with antenna arrays needs to address all the challenges related to size, cost, and performance [2]. These challenges translate to multi-layer fabrication with fine-line features, their process tolerances, precise layer-to-layer registration, advanced low-loss materials to reduce conductor losses, and co-simulation of circuit, device, package, and thermal solutions. The emerging 3D package integration solutions also underscore the need for isolation between the various circuit blocks. Because of the deployment of such high-power amplifiers and a large antenna array in millions of base-stations, cost needs to be addressed for high-volume manufacturing.

In addition to the large continuous bandwidth, the mm-wave band enables a highly-integrated and miniaturized 5G modules as most system components scale with the wavelength. The implementation of massive MIMO and hybrid beamforming for 5G mm-wave entails the use of antenna arrays and front-end transceiver ICs, with all integrated into a single package. Communications with 5G networks drive new packaging paradigms such as:

- Low-loss system interconnects with flip-chip assembly or wafer or panel embedding of phase shifters and beamforming ICs, transceiver ICs such as PA, LNA, and mixers
- Heterogeneous integration and interconnects for all the system elements - highly-integrated antenna packages interconnected altogether with transceiver ICs and passive components such as filters, where advanced packaging methodologies are strongly required.

1.1 Packaging Trends for 5G Systems

System-level packaging in the mm-wave technology should be partitioned into baseband modules and antenna-integrated transceiver modules. In such packages, interconnections between ICs and other elements such as antenna, passive components, and PCBs must satisfy several requirements. One of the most critical requirements is the impedance control especially in the analog domain. In the mm-wave antenna-in-package solutions, interconnections between transceiver ICs and antennas should result in low insertion loss and acceptable return loss over the frequency range of interest. The other key requirement is the form factor. Two types of interconnect techniques are widely available in the packaging industry, and a third technique has been rapidly emerging during the past decade. The two conventional techniques are wire-bonding (Fig. 1.2a) and flip-chip interconnections (Fig. 1.2b), whereas the emerging technique is referred to as IC-embedding or fan-out packaging (Fig. 1.2c). Although flip-chip and fan-out interconnections have originally been developed for high-performance computing (HPC) or mobile processor applications, their interconnection attributes such as fine pitch and low electrical parasitics are becoming critical in RF/mm-wave packages such as baseband modules and antenna-integrated modules.

Despite the maturity and cost effectiveness of the packaging industry, interconnection using the wire-bonding technique has been identified as one of the key challenges in realizing system-on-package (SoP) because of the significant signal loss and impedance discontinuity caused by the bond wire, which degrades the performance of the RF/mm-wave system chain [3]. Interconnects using the flip-chip technique offer better performance than wire-bonding as the bump height is smaller than the length of bond wires. The flip-chip technique is also preferable for small form factor and provides 800–10,000 inputs/outputs (I/Os). The flip-chip technique started with solder bumps with a diameter range of 75-200 μm, while copper-pillar interconnection with solder cap nowadays reaches down to the di-

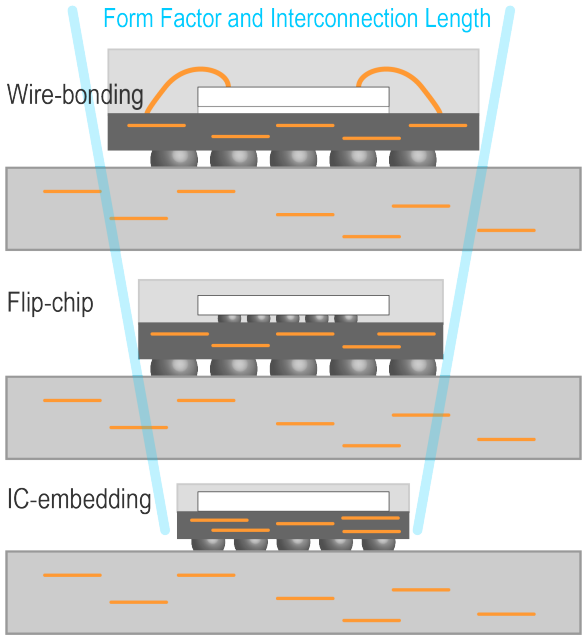

Figure 1.2: Trends of interconnection assembly methods in RF/mm-wave technology for miniaturization.

ameter less than 40 μm. The copper-pillar technique not only provides high-density I/O, but also offers lower conductor loss.

The recent evolution of IC-embedding or fan-out packaging has been imperative. Embedded wafer fan-out packaging, also referred as embedded wafer-level ball grid array (eWLB) pioneered by Infineon and fan-out wafer-level packaging (FOWLP) by others, offers several advantages for mm-wave packaging [4, 5, 6]. eWLB eliminates the use of wire bonding. This not only eliminates high-frequency loss and parasitics, but also reduces the package footprint for high-pin count die. In this approach, transceiver ICs are embedded in a reconfigured molded wafer with a compression molding process. Multiple redistribution layers (RDLs) are formed to fan-out the baseband signals, and through-mold vias are utilized for vertical interconnections. From the industry standpoint, Infineon, TSMC, ASE, Amkor, Deca Technologies, JCET, and several other companies have been leading the wafer-level fan-out technology for RF/mm-wave applications. In conjunction with the molding-compound-based waver-level IC-embedding technology, laminate-based and glass-based panel-level embedding technology is also emerging as an alternative candi-

date, mainly led by Samsung, Unimicron, ASE, and Deca Technologies from the industry, and Institute of Microelectronics (IME) [7] and Georgia Tech Packaging Research Center (GT-PRC) from the research standpoint [8, 9].

Fig. 1.3 illustrates the key modem and antenna-integrated packages. Most of these packages employ the combination of multiple techniques from the three interconnection methods. Bond wires could serve as interconnection between the PCB board and memory that is stacked atop the logic or modem die, while the modem die with high pin count entails flip-chip interconnects to provide clean signal and mitigated signal delay. The most popular assembly method to integrate a mm-wave phased antenna array with ICs interconnected is, as of now, the flip-chip technique because of the process cost and supply-chain maturity. Conductive materials are selected from copper pillar or C4 solder bumps, depending on the pin count and sensitivity of assembled dies to the conductor loss caused by interconnections.

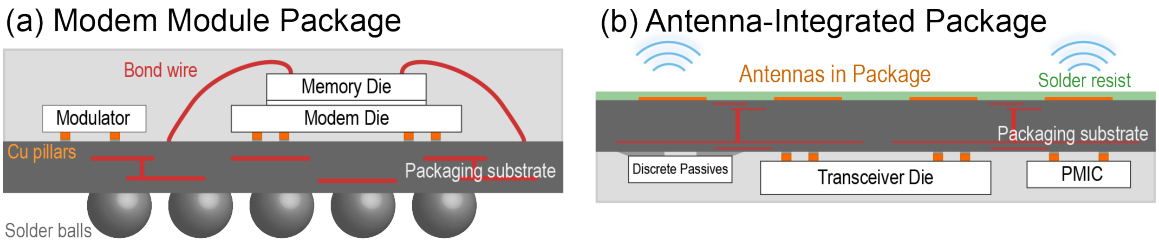

Figure 1.3: Examples of system-integrated mm-wave packages (a) modem SoP (b) antenna-integrated package.

1.2 Packaging Challenges in mm-wave 5G

High-density integration of mm-wave components for 5G RF front-end modules

5G mm-wave modules entail tight integration of antenna arrays, transceiver ICs, power-management ICs, the stacks of logic and memory, and surface mounted passive components, as depicted in Fig. 1.4. This reported thickness of mm-wave packaging substrates varies from 0.15 mm to 1.2 mm. The variation results mainly from the antenna-in-package

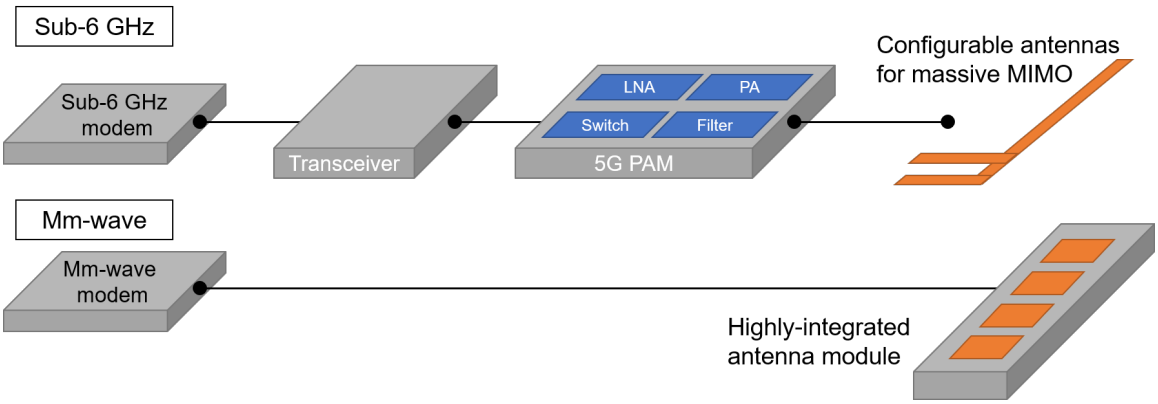

Figure 1.4: An example of tight integration in RFFE architectures for 5G electronics.

requirements. Packages without antenna could employ thin substrates below 300 μm. However, antenna-integrated modules require higher thickness as antenna arrays offer higher bandwidth with a thicker substrate due to more separation of ground planes from antenna patches. The thickness of entire modules (packaging-substrate thickness + mold height) also varies from 0.5 mm to 2 mm. In addition to the thickness requirement for antenna, the system components and interconnects (Fig. 1.4) determine the total thickness and the area of the entire packages.

Novel circuit design techniques

Integration of multiple components into a package requires more complicated signal routing and power delivery networks in a limited space, to attain the required signal and power integrity and the control of electromagnetic-interference (EMI). The dielectric thickness for signal routing and power distribution can be 15 μm and lower [8].

Multi-physics analysis and modeling

Ideally, devices, components, and interconnects should maintain stable performance under various signal, power, thermal and thermomechanical loads. As discussed in [10, 11], the packaging structure affects not only the signal and power distribution but also the electrical performance of each component or device. This demands accurate and reliable

multi-physics modeling and analyses for electrical, thermal and thermomechanical performances.

Co-Simulation of package, circuit and device

5G mm-wave technology entails co-design of phased antenna array with transceiver or beamforming ICs to meet the power distribution and signal integrity requirements, and passive components to support all the functions with minimal parasitics and interference. The co-design should also consider electromagnetic compatibility and thermal design, as exemplified by Gu *et al.* [12].

Novel Materials with good electrical and thermal properties

In conjunction with the traditional material requirements in IC packaging such as compatible CTE and Young's modulus, the new class of requirements especially for AiP leads to the development of low-loss dielectric materials. Low-loss materials mean materials with low dissipation factor, or loss tangent (tan δ). Low tan-δ mitigates dielectric loss in in-package interconnects, feedlines, and antennas, and thus increases the antenna efficiency. The high losses in the power amplifiers make thermal management more challenging. The recent notable material development is discussed in Section 2.1.1.

Process challenges for high precision patterning

Requirements for RFFE packaging differ from those for high-performance computing. RFFE conventionally prioritizes impedance control more than the high number of I/Os or the bandwidth of the interconnects. However, emerging heterogeneous-integration trend to support massive MIMOs will require finer-pitch I/Os between the chip, the package, or antenna array. It is, therefore, imperative to manage both impedance control and minimize tolerances in the manufacturing processes for small line width and spacing (L/S) down to 5/5 μm to 2/2 μm by 2025 and 1/1 μm by 2030. The emergence of AiP in front-end pack-

ages underscores the importance of multi-layer fabrication and layer-to-layer alignment with the precisely-controlled dielectric thickness. The fabrication accuracy of multi-layers is one of the key metrics to obtain good model-to-hardware correlation. Furthermore, metallization quality plays an important role. The surface roughness of the conductor degrades the signal quality, which needs to be incorporated in the process design to mitigate the system interconnect loss in conjunction with the effort to lower the dielectric loss.

Thermal management for 5G

Reduced separation distance between temperature-sensitive components and hot-spots, and the increased number of component density call for integrated heat-spreading structures from the thermal-management standpoint. 5G mm-wave technology is expected to consume more power than the previous generations of wireless technologies [13]. Efforts to address thermal-management challenges have been made both by the academia [14, 15] and industry [16, 12, 17] mostly with electrical and thermal co-design and analysis.

1.3 3D Glass-based Integrated RF/mm-wave Packages

3D integration of active and passive components has become the key strategy to realize high-performance millimeter-wave (mm-wave) systems for emerging 5G mobile communications. Innovative packaging architectures such as antenna-integrated modules are sought for all classes of 5G-enabling products such as handsets, customer premises equipment, and base-stations. From the system integration point of view, low interconnect signal losses from chip to antenna coupled with high-gain and high-bandwidth antennas are required to achieve superior system performance [18, 19]. Advanced packaging substrates and low-loss thin-film build-up dielectrics, co-design of actives, passives, antennas, and their 3D integration in mm-wave bands, are therefore widely pursued by the industry [20, 12, 21] and academia [22, 23, 24].

State-of-the-art packaging technologies in mm-wave modules include low-temperature

co-fired ceramic (LTCC) substrates [25, 26], low-cost PCB processes, advanced organic substrates [12, 27], and fan-out wafer-level packages (FOWLP) with epoxy molding compounds [4, 28]. LTCC substrates have advantages such as low-loss properties at high frequencies and low moisture absorption [29]. The limitation of the cost due to the difficulty in large-panel scalability of ceramic substrates, however, led to the prevalence of organic substrates [30]. Although LTCC substrates provide higher reliability, lower shrinkage, and smaller feature sizes [31] than multilayered organic substrates, the minimum line-and-space remains 40 μm due to the thick-film co-firing processes. In conventional laminate processes, copper foils or copper-clad laminates and prepreg are compressed to form low-cost multilayered organic substrates [21, 32, 33]. The main challenge is the limitation of small features (> 80 μm) caused by layer-to-layer alignment inaccuracy and substantive etching processes. The relatively coarse patterning leads to an increase in the metal layer counts. The through-hole vias are generally more than 200 μm, which hinders miniaturization and high-density packaging. In addition, these substrates cause warpage throughout the fabrication processes, which results in degraded electrical performance and reliability issues after the assembly of active and passive components. The most recent approach utilizes build-up layers on a rigid core substrate [23, 27]. High-density interconnects in build-up layers can potentially enable complex signal routing and reduce the metal-layer counts [8], leading to the thickness reduction of the entire modules. The elements accommodated in the package are interconnected with transmission lines, through-package vias, and microvias.

Figure 1.5 summarizes the advantages and disadvantages of each substrate technology. Organic substrates lead to several fundamental challenges in achieving high precision and tolerance below 5 – 10 microns. These attributes are important for precise control of impedance of high-frequency circuit elements [34]. Deviation from the desired dimensions induces frequency shifts and malfunction of such modules. Glass-based packaging has been drawing attention as an alternative solution to address these challenges in antenna in package (AiP) [35, 36] and integrated-passive devices (IPD) [37, 38], because of its ability

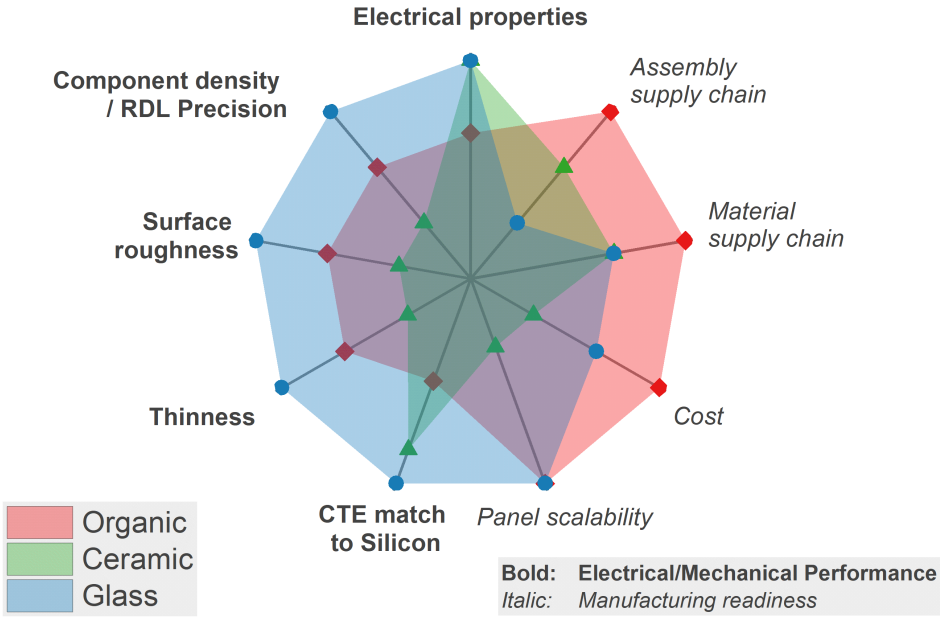

Figure 1.5: Comparison of three primary substrate materials used for 5G mm-wave applications.

to form fine-pitch line and spaces and through-glass vias (TGV) [8, 39, 40], dimensional stability, surface smoothness (< 10 nm), robustness against high temperature and humidity, matched CTE with silicon dies, and large-area low-cost panel-size processability [41, 42, 43]. It also features tailorability of dielectric constants (Dk) of 3.78 – 8 ppm/K and loss tangents (> 0.0003) [44, 45, 46]. CTE can be tailored between 3 to 8 ppm/K depending on the materials used for ICs and PCBs. These parameters provide electrical and mechanical engineers with more design flexibility [47]. However, one of the evident challenges is the lack of manufacturing readiness.

1.4 Research Objectives, Challenges and Tasks

1.4.1 Research Objectives

The objective of the research is to model, design, and demonstrate high-performance, and ultra-thin antenna-integrated 3D glass-based mm-wave packages. Two classes of unique challenges need to be addressed to realize ultra-thin 5G glass packages to achieve the ob-

jectives. Signal losses are aggravated because of the excessive attenuation at mm wave frequencies. Package integration with high component densities to incorporate all the system components such as antennas, transceiver ICs, filters, power dividers and combiners high signal routing densities. These interconnect layers need to comply with impedance-matched designs, adequate isolation and low signal losses.

Unique 3D laminated-glass packages are proposed to address these challenges and realize next-generation 5G system packages. Ultra-thin and ultra-low loss polymers on large ultra-thin glass substrates are proposed to achieve optimal combination of loss, process precision and multilayered wiring density, assembly and reliability for 5G packages. Glass, as a thin but high modulus core, provides exceptional dimensional stability, with minimum warpage that is required to achieve the 2% process precision across the panel. Glass panel is ultra-thin ($<$100 μm) and with ultra-smooth surface finish, unlike laminate cores. Its CTE (coefficient of thermal expansion) can be matched perfectly to Si but can also be optimized for both chip- and board-level reliability simultaneously. The performance superiority, however, comes from ultra-low loss dielectrics on the glass surfaces and around copper through-vias. Such a hybrid approach achieves ultra-low loss of PTFE–like materials (polytetrafluoroethylene), while improving RDL circuit precision by up to 10X compared to multi-layer organics. Through-package vias (TPVs) in glass can be scaled to 30–50 μm pitch, and even smaller in thinner glass substrates, compared to 300 μm or larger pitch in organic laminates and molded, embedded packages. The approach is also superior in reducing the size of the modules as it enables double-side integration and assembly of active and thin-film passive components with lowest loss, thus reducing the X-Y footprint of the modules by about half, and reducing the interconnect length between them to less than 100 μm. By scaling to 510 mm panel size manufacturing, the packaging can lower the cost compared to wafer-level packages.

The cross-section schematics of the antenna-integrated 3D glass-based mm-wave packages are illustrated in Figure 1.6. The left schematic in Figure 2 shows the *chip-last*

antenna-integrated packages. This architecture is preferred for high-power applications such as base stations that generate heat. The right schematic in Figure 2 is the *chip-fist* glass-panel embedding antenna-integrated package, where RF ICs are embedded in a cavity formed in a glass core substrate and interconnected to antennas and other elements through re-distribution layers.

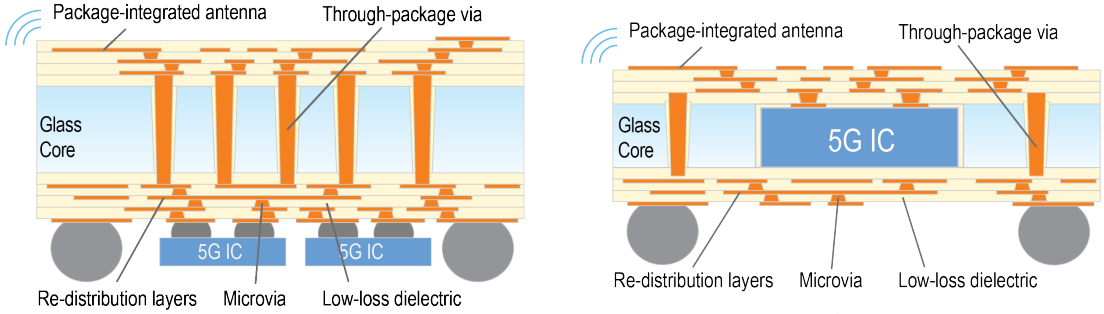

Figure 1.6: Glass-based 5G packages (a) Chip-last and (b) Chip-first configurations.

The key parameters of the proposed research in both packaging architectures (Figure 1.6) are listed in Table 1.1, comparing with those from other substrate technologies as prior art such as low-temperature co-fired ceramic (LTCC) and organic laminates.

1.4.2 Technical Challenges

Low-Loss High-Density Interconnects

Higher density and miniaturization of system components in the RF front-end are realized through an optimal combination of single-chip integration (System-on-Chip) and heterogeneous package integration of components (System-on-Package). Integrating all the system components into a single die, the SoC strategy, however, has several challenges to overcome because of complex design and design verification, low process compatibility, long time-to-market, and high development cost. The SoP strategy, in contrast, addresses the challenges with small form factor, design flexibility, and cost through 3D package integration of optimal SoC transceiver devices, passives, power dividers and antenna arrays.

Table 1.1: Research Objectives, Prior Art and Challenges.

Metrics		Objectives	Prior Art	Technical Challenge	Research Tasks
Performance	System interconnect loss	< 1 dB	3 – 4 dB	• Conductor and dielectric losses at 28 or 39 GHz. • Impedance discontinuity in vias	• Design and demonstration of low-loss TLs and SIWs
	Precision	2% with 50 µm	6 – 10 % with 80 µm	• Ultra-thin low loss materials • Process variations	• Performance impact of process variations
	Integrated-antenna bandwidth	24.5 – 29.5 GHz	26.5 – 29.5 GHz	• Low-loss dielectric	• Study on performance impact of process variations on antenna performance
Miniaturization	Module thickness	< 500 µm	> 800 µm	• Heterogeneous integration of components	• Heterogeneous integration of 5G components
				• Thick substrates	• Use of ultra-thin glass substrates
	Module footprint	X	2 X	• Signal-routing density	• High-density signal routing

One of the critical performance metrics in mm-wave SoP technologies is the signal losses because of the stringent link budget for low-power and long-range telecommunications. The losses originate from the increasing attenuation of electromagnetic waves in higher frequency bands. Both academia and industry have been exploring a wide variety of 3D package integration technologies to realize 5G communications. The key focus is the substrate integration of active dies, passive components, and antennas with the SoP strategy to compensate for signal losses caused by interconnects between components in a package. The highly-integrated packages with the SoP technology in the mm-wave spectra places more demands on the number of metal layers in a packaging substrate for signal routing, power or current distribution, and ground planes. Chip-last mm-wave modules with high-power and high-gain antenna arrays can require more than ten layers on the core substrate. The high layer count in 5G packages originate from the integration of several components such as assembled dies, passive components, signal and power planes, ground planes, an-

tenna array, and in-plane and out-of-plane electrical connections for signal and power distribution. Reduction of insertion losses and voltage standing wave ratio (VSWR) has been a key challenge in heterogeneous integration of mm-wave elements interconnected with in-package signal routings that include transmission lines, through-package vias (TPV), and microvias, which connect signal traces or planes in different layers. Technical challenges in these interconnects include high impedance matching to mitigate reflection loss and maximize the power transfer, and high precision of fabrication in the re-distribution layers [48].

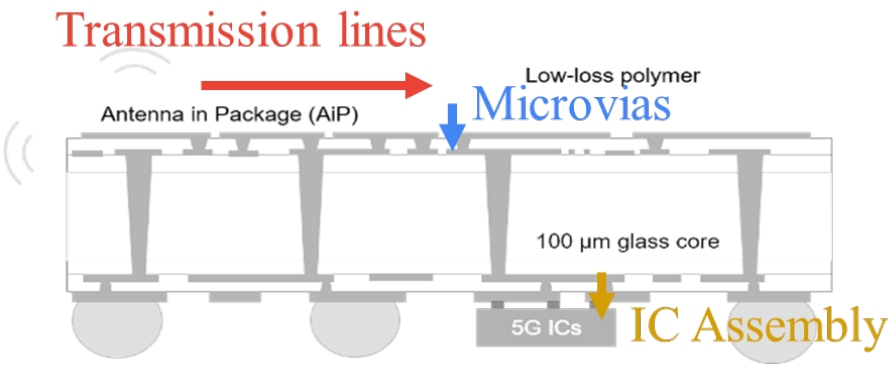

Figure 1.7: Comparison of three primary substrate materials used for 5G mm-wave applications.

Antenna-Integrated Packages

Systems with 5G connectivity impose several challenges associated with high-frequency designs, materials and processes, interconnect losses and process control necessary for precision impedance match. Distributed components with careful control in parasitics and propagation losses are needed. Miniaturized antennas with high bandwidth and gain are also needed. Current packages are based on ceramic substrates, organic laminates and fan-out packages with mold compounds. Ceramics are preferred because of their low loss, low moisture absorption, and stable properties in mm-wave range and manufacturing availability. However, the cost and integration limitations of ceramics led to the evolution of organic

packages. The evolution of embedded wafer fan-out packaging (EWFO), also referred to as embedded wafer-level ball grid array (eWLB) or fan-out wafer-level packaging (FO-WLP), further enhances the performance over organic mm-wave packages. In spite of these advances, current packages are limited in interconnect performance, component densities and integration capabilities.

Emerging wafer fan-out packaging utilizes mold compounds with high dielectric losses, high moisture-uptake and temperature-sensitive properties. The interconnect and components losses reported with these approaches range from 2–4 dB as reported in a recent study by TSMC [28], which do not meet the proposed performance metrics in this thesis. The poor dimensional stability, which leads to low precision circuitry of organic laminate and fan-out packages is a major concern to be overcome with any new package technology. Emerging approaches such as organic laminate panel-embedding or FOWLP do not provide enough process stability and process control necessary to achieve fine features with high precision, which is a key challenge for 5G. A recent report by ASE shows single-polarization antenna-integrated packages in $16 \times 8 \times 0.4$ mm^3 size to achieve adequate antenna gain of 12–14 dBi [49]. The large CTE mismatch between the device and packages also generates large interfacial and interconnect stresses, leading to mechanical reliability challenges. The large stand-off heights required for component assembly also increase the overall system losses. Interconnect heights of 80 μm for off-chip interconnections and 250–400 μm for board level assembly are required to achieve adequate reliability. Current approaches cannot simultaneously meet all these needs for high-I/O density and high precision wiring density with ultra-low loss interconnects. A new class of substrate technologies are needed to comprehensively address all these challenges and realize next-generation 5G systems.

1.4.3 Research Tasks

High-performance 3D Antenna-Integrated mm-wave Packages

Tight integration of mm-wave elements and components such as antenna array and filters into 5G RF front-end modules and interconnecting them are interdisciplinary challenges. The first set of research tasks include fundamental studies in low-loss, high-density chip-to-antenna interconnects in the mm-wave frequency spectra. These interconnects include microvias, substrate-integrated waveguides, and transmission lines on glass packaging substrates and re-distribution layers laminated on the glass cores. The electrical performance of through-glass vias is well studied in [50]. The interconnects are designed at circuit-level and with 3D full-wave electromagnetic simulations, fabricated through optimized processes, and characterized with high-frequency characterization.

Based on the fundamental research on low-loss high-density interconnects, the second part of the research tasks include the design and demonstration of the high-performance ultra-thin 3D glass-based mm-wave antenna packages. The 3D 5G antenna package consists of a thin glass core and low-loss dielectric thin-films with double-side routing and multi-layered interconnects. It is critical to design and simulate low-loss interconnects from chip to antennas for the multi-layered stack-up on thin glass substrates, along with the integration of antenna, filters, active ICs, and passive components. The design and demonstration of ultra-thin glass-based mm-wave packages in this research employ both a) chip-last or b) chip-first package configurations, as illustrated in Figure 1.6.

Glass Substrate Fabrication with Precise RDLs

Conventional low-cost PCB-like processes employ subtractive etching to pattern metal traces on copper-clad laminates (CCL) and prepregs that are pressed altogether to form a multi-layered package [21, 22]. Due to the limited layer-to-layer alignment accuracy during the thermal compression process, the PCB-like processes with low-loss organic ma-

terials offer minimum features of 40 μm. The limitation of the process tolerance entails relatively-large landing pads for through-package vias (TPVs) causing impedance discontinuity between signal traces and vias. However, the semi-additive patterning (SAP) processes on silicon or glass substrates, which are primarily used for high-performance computing applications to interconnect logic and high-bandwidth memories, generally lead to high precision of metal patterning with 2–5 μm line-and-space [51, 52]. The small-feature and high-density trend is also becoming more critical for highly-integrated 5G mm-wave packages. The high-density packages, shown in Figure 1.8, also lead to the reduction of required metal-layer counts, the mitigation of package loss, undesired parasitics, and the total thickness of antenna-integrated packages.

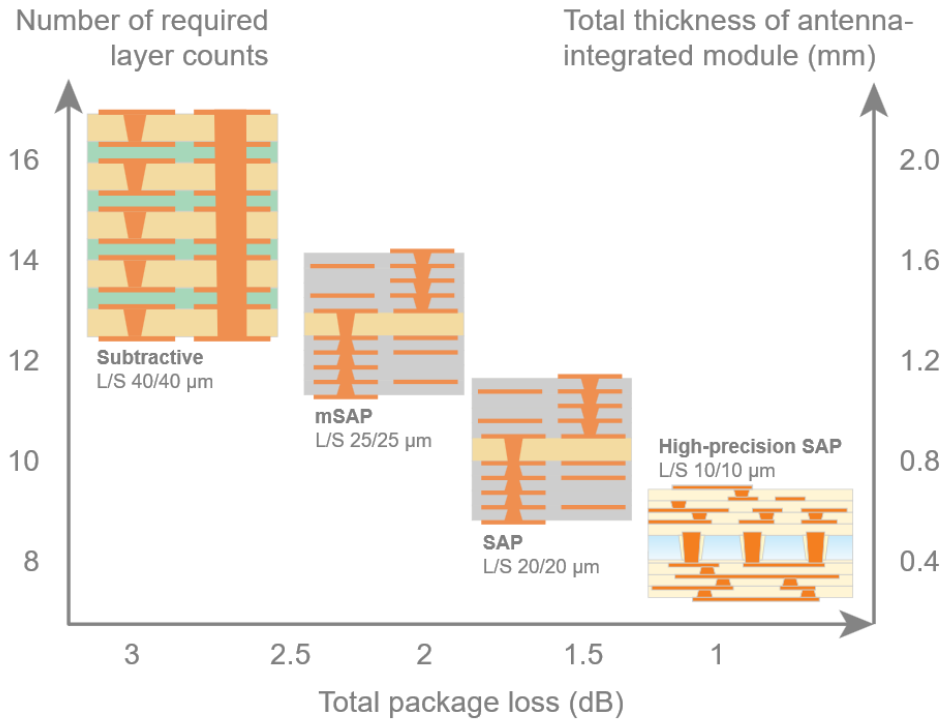

Figure 1.8: High-density and miniaturization trend for 5G highly-integrated mm-wave packages.

However, one of the challenges in achieving such small features ($<$ 20 μm) on thin substrates ($<$ 300 μm) is process-induced variations at each fabrication stage and their

impact on the electrical performance. Large process variations result in deviated frequency responses from designs and malfunctioning of mm-wave elements or components. Experimental characterization results such as dielectric thickness, conductor thickness and dimensions, and layer-to-layer registration need to be documented, and refined electrical models have to be built with actual geometries. To show the capability of glass substrates with laminated low-loss dielectric layers, the research tasks include precise fabrication of mm-wave elements and components and the comparisons of simulation results of the new model with measurement results on fabricated samples.

1.5 Dissertation Organization

The chapters are organized as follows. Chapter 2 compiles the literature survey of 5G mm-wave packaging technology. Chapter 3 discusses the fundamental research on low-loss high-density package-level interconnects in mm-wave frequency bands. Chapter 4 presents the design and demonstration of the two types of packaging configurations for 5G mm-wave glass-based packages. Finally, Chapter 5 summarizes the overall research results achieved, major scientific and engineering contributions, and suggestions for future work.

CHAPTER 2
LITERATURE SURVEY

In order to meet the emerging needs for mm-wave modules, major advances are being made in devices, system design, and package-integration technologies. Both academia and industry have been exploring a wide variety of package integration technologies to realize 5G communications, with specific emphasis on 3D system integration technologies with low-loss interconnects and higher antenna gains to address the path losses in mm wave frequencies. This chapter reviews the recent advances that address the challenges such as increased substrate loss, dominating role of interconnection parasitics, and reduced radiation efficiency of antenna arrays in mm wave frequency bands.

2.1 Low-loss High-Density Interconnects

2.1.1 Development of Low-Loss Dielectric Materials

The selection of dielectric materials is critical to obtain the desired electrical performance of ICs and antenna arrays integrated in 5G module packages. A wide variety of dielectric materials are investigated to meet the requirements for various applications such as handset devices, radar modules, base-stations, and satellites. Low-loss dielectric materials provide improved link budget, low signal dissipation, high signal or power density, desired frequency response of passive components, small footprint of elements, lower module thickness, high antenna efficiency and EIRP, beam width, angular coverage, energy consumption, and miniaturization of antennas.

LTCC (low-temperature co-fired ceramic) substrates facilitated initial advances in RF substrates because of their ability to integrate complex 3D multilayered conductor patterns with through and blind vias. Progress in RF passives started with LTCC, which became

very popular for RF discrete and integrated surface-mount technology (SMT) components. They have been employed for high-frequency antenna modules such as WiGig, alternatively known as 60 GHz WiFi, which includes IEEE 802.11ad standard and also the upcoming IEEE 802.11ay standard. The large number of metal layers and relatively-low tan δ are the major advantages of LTCC substrates, as indicated in Table 2.1. Their low coefficient of thermal expansion (CTE) and high thermal conductivity also lead to high reliability and robustness to temperature variations. The major challenges are the low density of signal routings in internal layers and size scalability. As LTCC substrates are fabricated with screen-printing and co-firing processes, the RDL features are generally large (> 125 μm) due to the dimensional limit of screen-printing masks and alignment accuracy between layers. This large feature size results in low density of signal routing and entails high number of metal layers.

The mainstream platform for antenna integrated packages is still based on multi-layered organic substrates. The process for the multi-layered organic substrates for mm-wave modules is similar to that of PCB manufacturing and is cost-effective due to the compatibility with the existing supply chain and high-volume manufacturing for consumer electronics. Organic materials are designed to show lower tan δ, compared to the traditional FR4, where tan δ is higher than 0.02 in the mm-wave frequency bands. The mainstream copper-clad laminates (CCL) and prepregs used for formation of multi-layered organic substrates comprises of four classes of polymers: 1) Bismaleimide Triazine (BT), 2) Polyphenyleneether (PPE), 3) Liquid-crystal Polymer (LCP), and 4) Polytetrafluoroethylene (PTFE), as listed in Table 2.1. Unlike glass-cloth epoxy resin (e.g., FR4), glass-cloth PPE substrates feature high glass-transition temperature (Tg), low water absorption, low dielectric constant (both Dk and Df). PPE-based substrates are typified by MEGTRON6 (core and prepreg) from Panasonic, and CS-3376C from Risho Kogyo. Similar to PPE resin, the lamination of BT-based core with build-up dielectrics form the multi-layered organic substrates. BT-based laminates provide low CTE, low shrinkage, and high peel strength with copper. LCP and

Table 2.1: Low-loss dielectric materials recently used for 5G substrate technology

	Materials	Dk Df ($\times^{-4}$)	Reported frequency	Major suppliers
Organic	Bismaleimide Triazine (BT)	3.4 40 – 50	10 GHz	Mitsubishi
	Polyphenyl-ethers (PPE)	3.25 – 3.4 20 – 50	1 – 50 GHz	Panasonic, Risho Kogyo
	Liquid-crystal Polymer (LCP)	2.9 25	10 GHz	Rogers, Murata
	Polytetrafluoro-ethylene (PTFE)	2.2 9	10 GHz	Rogers, DuPont
Inorganic	Low-temp. cofired ceramic (LTCC)	6 18	60 GHz	Hitachi Metals, Kyocera, TDK
	Borosilicate glass	5.4 50 – 90	10 – 60 GHz	AGC, Corning, Schott, 3DGS, NSG
	Fused silica	3.8 3 – 4	10 – 60 GHz	AGC, Corning, Schott, 3DGS, NSG

PTFE are gaining attention because of low tan δ at the mm-wave frequency range. Unlike PPE and BT, these materials require high-temperature and high-pressure processes for lamination and thermal compression. Halogenated substrates are not usually preferred for handset applications for environmental and safety concerns.

The mechanical and process limitations of organic laminates from their low modulus and high CTE are addressed with emerging inorganic substrates, as listed in Table 2.1. Glass substrates offer a wide range of Dk (3.7 – 8) and Df (0.0003 for fused silica to 0.006 for alkaline-free borosilicate), smooth surface, good dimensional stability ($< 2\mu$m for 20-mm substrates), large-panel scalability, ability to form fine-pitch through vias, stability to temperature and humidity, and tailorable CTE depending on the packaged components [44, 43, 47, 8, 53]. Companies such as Samtec and Unimicron manufacture glass-based

packages. However, glass-based packaging still poses challenges associated with process immaturity and higher cost resulting from lack of the manufacturing readiness and the nature of glass such as brittleness and difficulty in handling.

In conjunction with the substrate materials, the formation of RDL and microvias [45] becomes more critical to form high-density interconnects ($< 10\ \mu$m) and to enable tight integration of components. Dry-film dielectric materials show good compatibility with panel-level packages with double-side RDLs and offer a wide thickness variation ($> 5\,\mu$m). Low-loss or low tan δ materials are developed in the industry for recent mm-wave packages, as shown in Table 2.2. Low-loss dry-films, which are typically epoxy-based, usually contain silica or ceramic fillers to lower the dissipation factor (tan δ). The fillers increase Young's modulus, decrease CTE, but lead to technical challenges from the narrow process window, poor adhesion to substrate materials, and reliability in harsh environment. The other method to form dielectric is the use of liquid-based dielectric such as polyimides. As opposed to dry films, liquid-based dielectric materials are more compatible with wafer processes or build-up layers on one side of the substrate. Non-filler photo-sensitive or photo-imageable low-loss liquid-based dielectric materials designed for 5G mm-wave applications are emerging to form fine features below 5 μm [54, 55, 56]. Low-loss liquid-based dielectric materials from major suppliers are listed in Table 2.3. These materials are, however, not still in high volume manufacturing phase. The other challenge is that these materials are spin-coated or slit-coated and have difficulty in forming films with thickness more than 40 μm.

Table 2.2: Low-loss build-up dry films for high-density signal routings for high-frequency applications

	Dk	Df ($\times 10^{-4}$)	Frequency	CTE (ppm/K)	T_{g} (°C)
Ajinomoto	3.3	44	5.8 GHz	20	153
DOW	2.57	32	1 MHz	63	250
Hitachi Chem.	3.3	34	5 GHz	17	233
Sekisui	3.3	37	5.8 GHz	27	183
Taiyo Ink	3.3	25 – 30	5 – 60 GHz	20	160

Table 2.3: Low-loss photosensitive (photo-imagable) dielectrics for high-density signal routings for high-frequency applications

	Dk	Df ($\times 10^{-4}$)	Frequency	Min. L/S	Elongation (%)
DOW	2.65	8	<20 GHz	18 μm	8
Hitachi Chem.	2.4	18	10 GHz	–	–
JSR	2.6	48	< 40 GHz	8 μm	> 50
Toray	2.9	30	1 GHz	30	–

2.1.2 Transmission Lines

In 5G mm-wave packages, several transmission lines are commonly used depending on the performance and system design, and integration constraints. These include microstrip, stripline, co-planar waveguides (CPW), conductor-backed CPW (CPWG), as illustrated in Figure 2.1. While the microstrip and striplines are preferred for high-density signal routings due to the absence of in-plane ground [57], CPW and GCPW are more common in multi-layered packages for 5G mm-wave packages because of their inherent shielding features and minimal cross-talk with other nearby transmission lines or components. In mm-wave frequencies (20 GHz and above), dielectric loss is dominant in multi-layered signal routing, resulting in a high demand for low-loss-tangent (tan δ) dielectric materials to maintain the signal integrity and mitigate signal losses in a package.

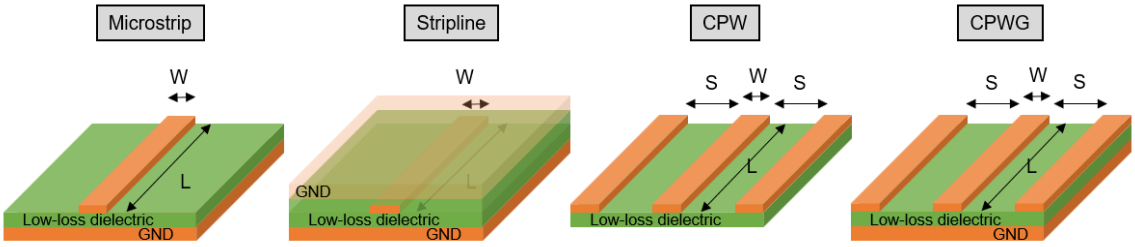

Figure 2.1: Chip-last 5G antenna-integrated package with a glass core, low-loss laminated polymer for RDL, TPVs, microvias, and IC assembly, and ball-grid arrays.

2.1.3 Microvias

One of the most critical performance metrics in mm-wave SoP technologies is the signal losses because of the stringent link budget for low-power and long-range telecommunications. The losses originate from the increasing attenuation of electromagnetic waves in higher frequency bands. Both academia and industry have been exploring a wide variety of 3D package integration technologies to realize 5G communications. The key focus is the substrate integration of active dies, passive components, and antennas with the SoP strategy [8, 27, 21, 58] to compensate for signal losses caused by interconnects between components in a package. The highly-integrated packages with the SoP technology in the mm-wave spectra places more demands on the number of metal layers in a packaging substrate for signal routing, power or current distribution, and ground planes. Chip-last mm-wave modules with a core substrate typically require more than ten layers [27, 59], as shown in Figure 2.2. This requirement comes from the integration of higher number of elements such as assembled dies, passive components, signal and power planes, ground planes, antenna array, and in-plane and out-of-place electrical connections for signal distribution. In-package signal routing includes transmission lines, through-package vias (TPV), and microvias, which connect signal traces or planes in different layers.

The electromagnetic waves attenuate as they travel through each interconnect path such as transmission lines, TPVs, interconnection bumps, and microvias [60, 61]. Studies have been performed to reduce the losses caused by transmission lines and TPVs [62, 63, 64, 65] as they are the major cause for the signal attenuation. Microvia losses have not been investigated as they are negligible in sub-6 GHz [66, 67]. In the mm-wave frequency bands, however, the microvia losses must be mitigated as the electrical length of microvias increases with the increasing frequencies and the increasing number of metal layers in a single package [68, 69]. Suitable design of microvia geometries can minimize such interconnect losses to minimize the transition losses and enable seamless mm-wave transitions.

In conventional radio-frequency (RF) front-end packages that cover up to 5 GHz, in-

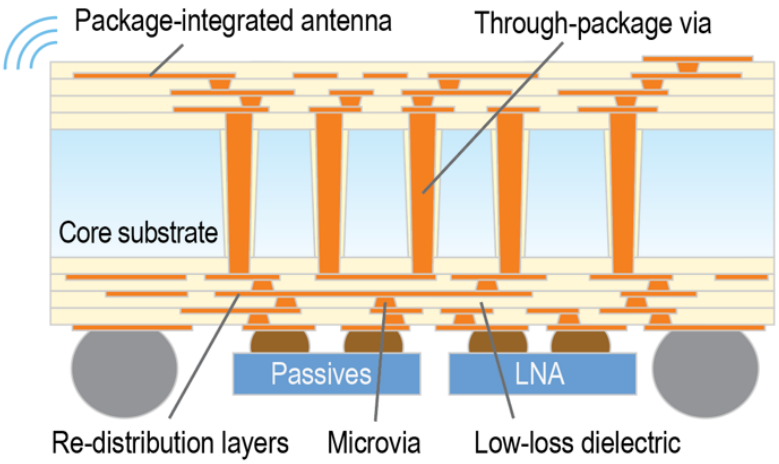

Figure 2.2: Chip-last 5G antenna-integrated package with a glass core, low-loss laminated polymer for RDL, TPVs, microvias, and IC assembly, and ball-grid arrays.

terconnecting microvia sizes range the diameter of 40 – 200 μm while the width of transmission lines (e.g., microstrip lines, co-planar waveguides, striplines) spans greater than 40 μm. This large diameter of microvias and the high transmission-line widths depend on the thickness of dielectric layers, which range 40 – 100 μm. As shown in Figure 2.3,

The width of a 50-Ω impedance-matched microstrip-line has a linear correlation with the thickness of inter-layer dielectric. This relation is shown in Figure 2.3. Thicker dielectric layers of 40 – 100 μm result in large diameter of microvias and the high transmission-line widths. In conventional RFFE packages that cover up to 5 GHz, interconnecting microvia diameters range from 40 μm to 200 μm while the width of transmission lines (e.g., microstrip lines, co-planar waveguides, striplines) spans greater than 40 μm. With the recent advances in the reduction of dielectric thickness in build-up layers to below 40 μm, transmission-line width can be reduced while maintaining the standard impedance of 50 Ω, 75 Ω, or 100 Ω. The reduction of transmission-line width brings about high-density signal routing and of the need for small microvias for seamless transitions from transmission lines to microvias and vice versa. The geometrical difference between the transmission-line width and microvia diameter causes electromagnetic discontinuity and thus higher signal reflection. The seamless signal transition with suppressed signal reflection is enabled by

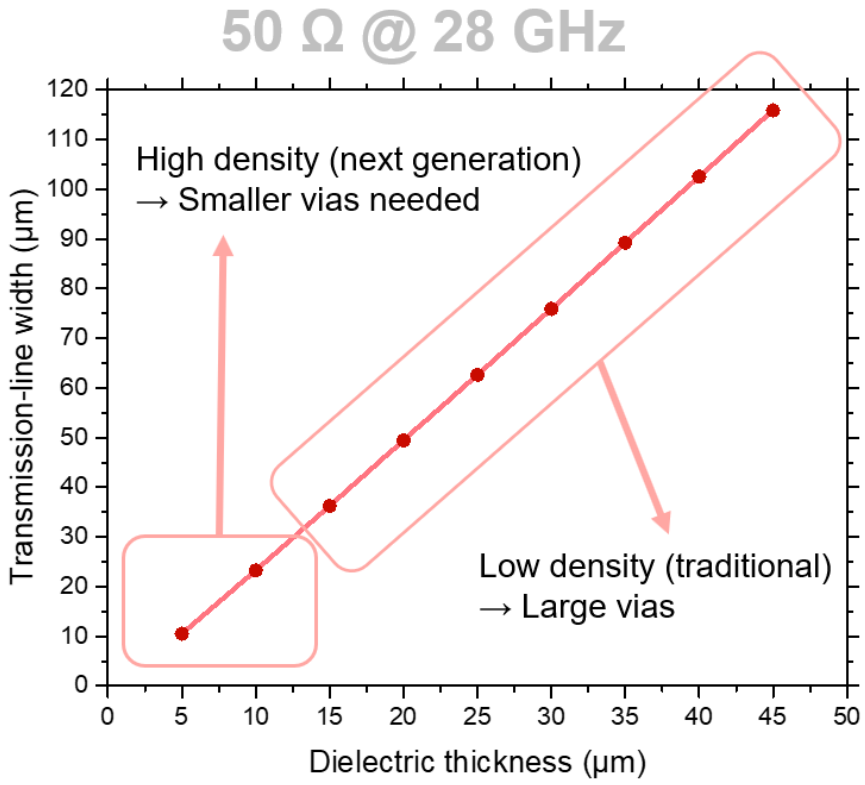

Figure 2.3: Dimensions of a 50-Ω impedance-matched microstrip line at 28 GHz for the current specification and the next-generation high-density signal routing.

small microvias.

2.1.4 Substrate Integrated Waveguides

To address the challenges such as signal loss, electromagnetic interference, size reduction with direct antenna-integrated packages, and thickness reduction, substrate-integrated waveguide (SIW) strategy is gaining attention for low-profile waveguides fabricated into a dielectric substrate, as shown in Figure 5. This approach realizes package-integrated antennas, antenna feedlines, band-pass filters, power divider, and other passive elements.

Conventional methods utilize organic substrates such as liquid-crystal polymer (LCP) [70], hydrocarbon ceramic [71], and polytetrafluoroethylene (PTFE) [72, 73] because of their large-area low-cost manufacturing infrastructure cost and low dissipation factor [15]. These substrates, however, lead to several fundamental barriers and challenges to achieve

Table 2.4: Comparison of the insertion loss of SIW with various packaging substrates.

	[70]	[71]	[72]	[73]
Material	LCP	Hydrocarbon ceramic	PTFE	PTFE
Dielectric constant, ε_r	3.16	3.38	2.2	2.94
Dissipation factor, tanδ	0.0049	0.0027	0.0009	0.0012
CTE (ppm/K)	17	40	125	12
Thickness (μm)	127	1524	254	508
Frequency (GHz)	50–70	7–14	50–75	50–75
Insertion loss (dB/mm)	0.12	0.038	0.042	0.035

high precision and tolerance that are required for mm-wave components in the dimension of a few microns. The reported work with traditional organic substrates is summarized in Table 2.4.

2.2 Antenna-Integrated mm-wave Packages

2.2.1 Antenna in Packages

The 5G wireless communication system entails highly-integrated radio access solutions, incorporating advanced phased-array antenna and transceiver front-end technology to support high radiated power, large signal-to-noise ratio, as well as beamforming, scanning in elevation and azimuth directions within a wide range [12, 74]. As the antenna element size and pitch are correlated with the wavelength, antenna-in-package solutions become more feasible at mm-wave frequencies unlike discrete antennas for 4G/LTE. Major package-integrated antenna structures are patch antennas and dipole antennas. More number of antenna elements (N) results in additional gain ($10 \log N$). A 2 $\times$ 2 antenna array in Qualcomm QTM052 is reported to have a gain of 20 dBi, which comprises of 5 dBi per element, 6 dBi from summation, 6 dBi from array formation and additional 3 dBi gain from single polarization.

Patch antennas feature the main lobe in the elevation direction and enable dual-polarization which increases the channel capacity. The size of a patch-antenna array is approximately $\lambda/2$ (effective half wavelength on dielectric) with a pitch of $\lambda_0/2$ (half-wavelength in air).

These fundamental design rules lead to the requirement of high-Dk materials for miniaturization. High-Dk materials, however, degrade the bandwidth and gain. The thickness or separation of the patch and ground is critical since the antenna bandwidth increases almost linearly with the thickness. Another technique to increase bandwidth is the stacked-patch antenna. The stacked patches create two resonances at different frequencies, which also calls for high accuracy of layer-to-layer alignment to obtain the desired frequency responses. Antenna designs are performed considering the trade-offs between the size and performance (i.e., bandwidth and gain). Common feeding methods are the via-feed or aperture-coupling feed. Via-feeding is relatively simple and guarantees the accuracy of feeding points into the antenna patch. However, the challenge is the limited bandwidth because of the inductive reactance caused by the via [75]. Conformal via shielding is employed to emulate coaxial feed to reduce the undesired inductance and enable better impedance matching. In contrast, aperture-coupled feed leads to higher bandwidth than the via feed, while the layer-to-layer alignment is extremely critical; a few-micron shift between layers causes the frequency shift and may result in not covering the targeted frequency bands.

Dipole antennas are employed for covering the azimuth direction with a single polarization. Since the length of the dipole is nearly $\lambda_0/2$, the design process is relatively simple. Dipole antennas generally offer wide bandwidths, compared to patch antennas. The gain is controlled by placing additional number of directors in a modified antenna topology referred to as Yagi-Uda antenna. Dipole antenna and Yagi-Uda antenna are fed by two differential transmission lines to reverse the phases of the provided signals. Co-planar-waveguide and stripline signal routing are more common in multi-layered packages because of their inherent shielding features and minimal cross-talk with other nearby transmission lines, components, and antennas.

There are several options to implement mm-wave antenna array, as shown in Fig. 2.4. The first option refers to implementing antennas directly on the PCB board (Fig. 2.4a) [76,

33, 21]. The most notable advantage is the lower cost than the other options because of the supply-chain maturity. The major challenges of antenna on PCB are manufacturing process and tolerances. The relatively-coarse design rules do not allow designers to layout fine structures in transmission-line widths, spaces, via diameters and pitch, and accurate layer-to-layer alignment. Fig. 2.4b illustrates the most viable option for 5G mm-wave applications, the implementation of AiP. In contrast, Fig. 2.4c shows the direct antenna implementation onto the IC wafer. Although the antenna-on-chip approach offers the lowest feed-line loss and parasitics and provides direct integration with other front-end circuitry [77], the challenges include antenna efficiency, process scalability for large array, yield and cost, thermomechanical reliability issues, and design flexibility.

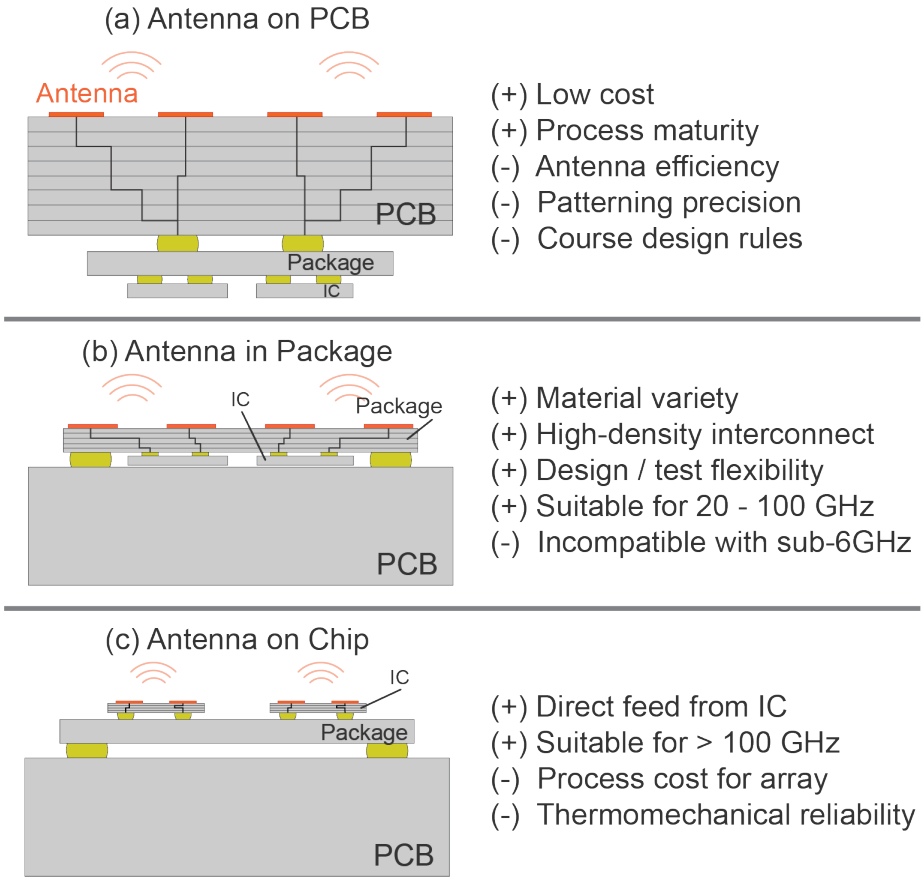

Figure 2.4: Three approaches for mm-wave antenna implementation. (a) Antennas on PCB, (b) antennas in package, and (c) antennas on chip or wafer.

2.2.2 Antenna-Integrated mm-wave Packages

This section introduces heterogeneous package integration for mm-wave antenna-integrated packages. Recent mm-wave antenna-integrated packages are classified into two categories based on interconnection techniques: a) chip-last or flip-chip structures, as shown in Fig. 2.5a and b) chip-embedded structures exemplified in Fig. 2.5b. System-level architectures and applications are discussed along with the packaging structures and materials in Section 2.1.1.

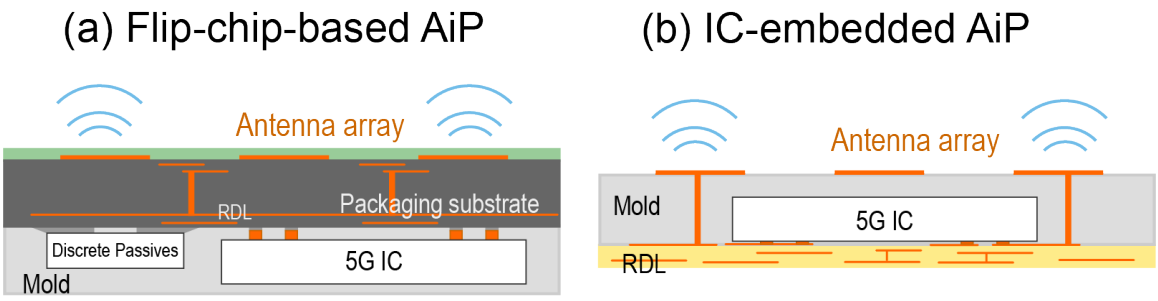

Figure 2.5: Packaging structures for antenna integration (a) currently-viable flip-chip-based configuration (b) IC-embedded configuration.

IBM made pioneering advances in AiP with organic laminate substrates for base stations, as shown in Fig. 2.6. The multi-chip antenna-in-package includes 64-array embedded antennas with dual-polarized operation in Tx and Rx modes, with four transceiver ICs that are assembled on the backside with flip-chip technology. In addition, to ensure thermal management, a heat sink is added to ball-grid array (BGA) interface, which allowed to realize consistent board-level assembly. This module operates at 28 GHz and achieves more than 50 dBm EIRP in Tx mode and $\pm 40^{\circ}$ scanning range with $70 \times 70 \times 2.7$ mm^3 [12, 79]. Ericsson developed similar AiP to implement a reference design for base stations. UCSD also reported 64 dual-polarized dual-beam single-aperture 28-GHz phased array for 5G MIMO, which is implemented in low-cost organic laminates. A 2×4 dual-beam former chip is flip-chip assembled on the other side of the antenna array. The array achieved an EIRP of 52 dBm at 29 GHz and scanned $\pm$ 50° and $\pm$ 25° in azimuth and elevation planes,

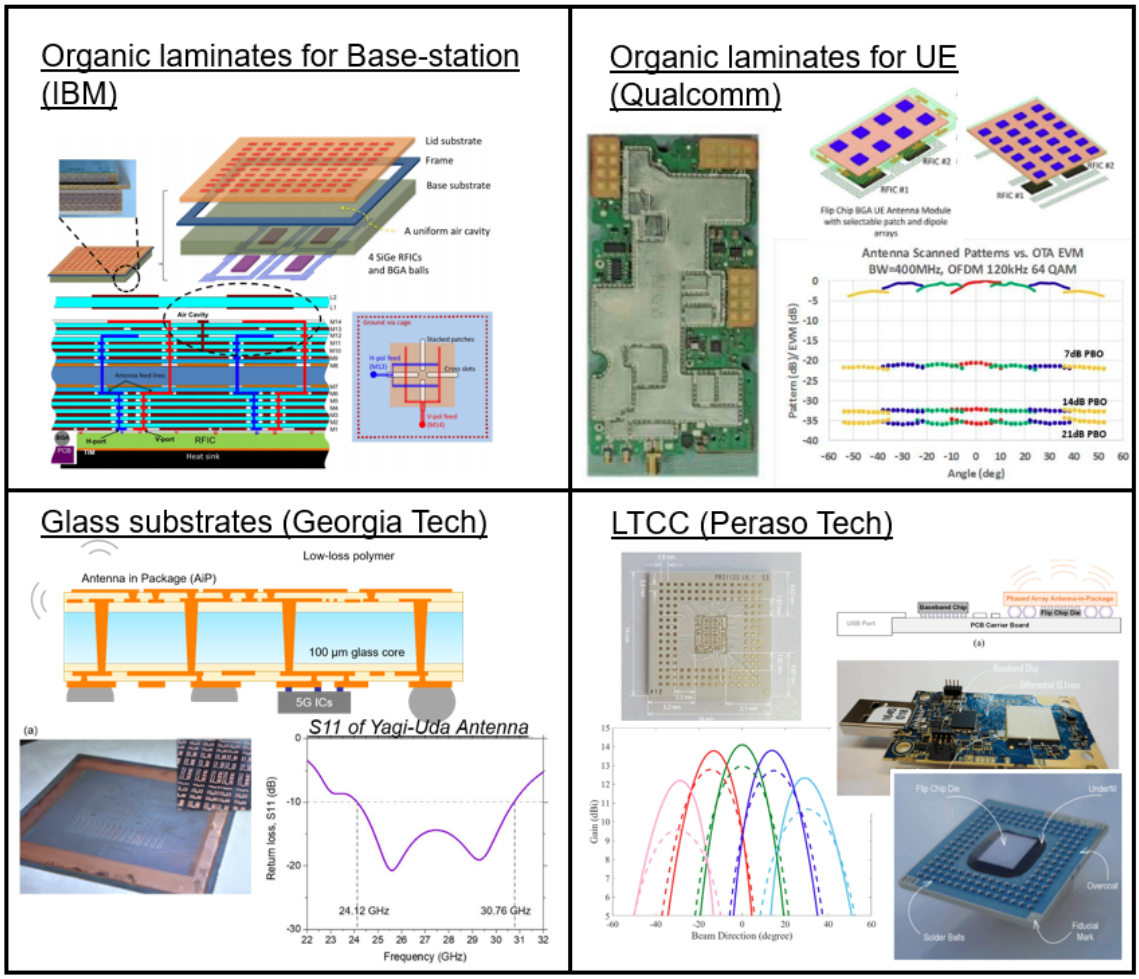

Figure 2.6: Demonstrated mm-wave modules with flip-chip-based AiP: organic laminates from IBM [12] and Qualcomm [20], glass-based substrates [8], and LTCC [78].

respectively, with cross-polarization rejection $>$ 30 dB [22].

Intel [21] has reported a stack-up that consists of an organic laminate-prepreg core for antenna implementation, trace routing, a flip-chip RFIC module that is responsible to quad-feed the antenna, where each port is responsible for one band and polarization, and BGA for connection to the main PCB, along with conformal shielding. The package size is 30 $\times$15$\times$1.5 mm^3, with 1500 connections for each transceiver IC feeding an 8$\times$4 patch antenna arrays to support linear dual-polarization with 20 dB isolation and dual-frequency antennas. This work includes the validation of the design and packaging concept suitable for low-cost 5G mm-wave CPE and base-station applications. Qualcomm has been

pioneering 5G UE modules with ICs in pair with 1×4 dipole, 1×4 patch, 2×2 patch, and 2×4 patch antenna arrays [20]. The second generation of their antenna SiP module covered dual-band (28 and 39 GHz) operation with the size of 19.1×4.9×1.78 mm^3. The antenna module includes power-module IC and transceiver IC, which are flip-chip assembled on the other side of the antenna patterns with copper pillars.

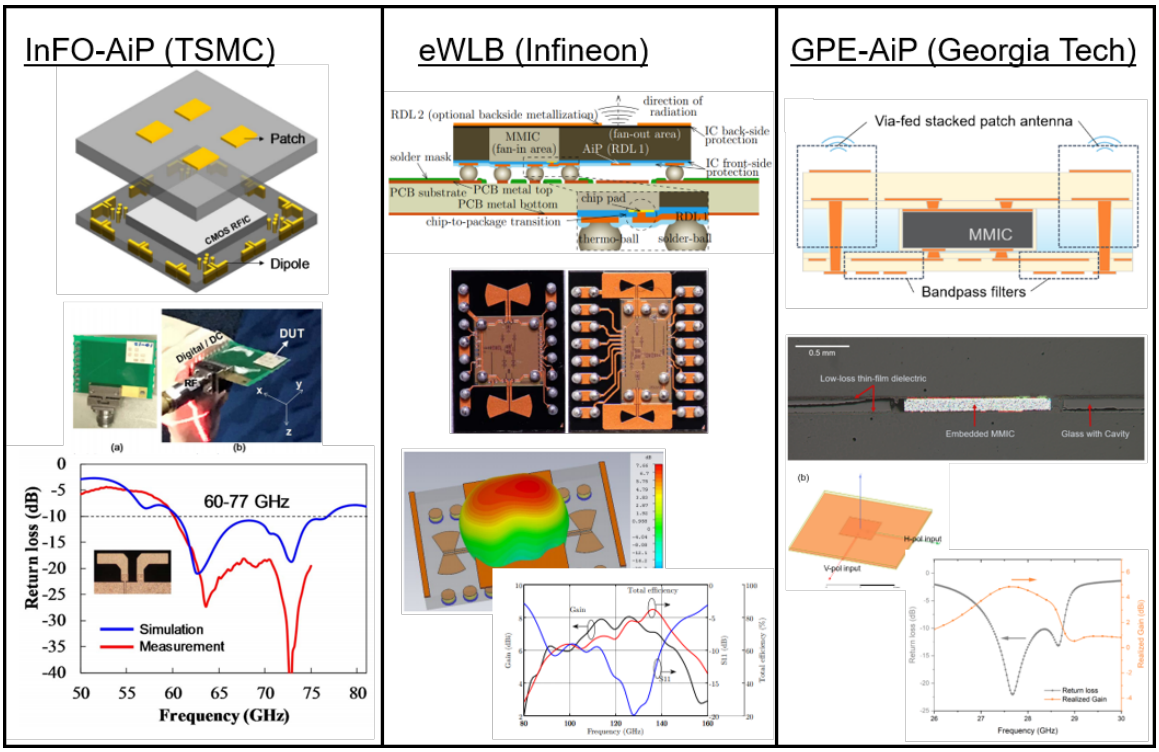

Figure 2.7: Demonstrated mm-wave modules with IC-embedded AiP: molding-compound-based InFO-AiP from TSMC [80], eWLB from Infineon [81], and glass-based [82] fan-out or chip-embedded packaging structures.

As one of the earlier demonstrations for AiP, a 60-GHz antenna integration with transceiver chips in a multi-layer LTCC were achieved by NEC Corporation, IBM [83, 84], Samsung [85], Intel [86], and a few more companies. Recently, Peraso Technologies Inc. in conjunction with Hitachi Metals Ltd. [78] introduced novel corrugated soft or high-impedance surfaces and implemented them between phased-array antenna elements in LTCC procedure for 5G mm-wave communications. Their array preserves 14 dBi gain with 8 elements and 16.5 dBi gain with 16 elements over a 10-GHz bandwidth around 60 GHz. Glass-

based AiP is also widely investigated especially in recent years [8, 35, 53, 87, 88], because of its potential of electrical properties, dimensional stability, and panel scalability toward 500×500 mm^2. In 2020, Singh *et al.* from Nokia Bell Labs [89] presented the demonstration of a D-band radio-on-glass module for spectrally-efficient (up to 521-QAM) and low-cost wireless backhaul, in which the module consists of two highly-integrated SiGe BiCMOS transceivers with a record low-loss glass interposer technology. The covered frequency bands are 115 – 155 GHz and 135 – 170 GHz. Similarly, Elkhouly *et al.* [90] again from Nokia Bell Labs reported wide-band TX and TX phased-array front ends for D-band (130 – 170 GHz). The presented waveguide-integrated low-loss glass interposers were manufactured by 3D Glass Solutions, Inc [91].

For next-generation AiP, chip-embedded structures are promising for form-factor and thickness reduction with shorter interconnects, as shown in Fig. 2.7. Infineon pioneered the fan-out wafer-level packaging (FOWLP) technology with their eWLB and reported antenna-integrated package in 2012 [4]. Advanced Semiconductor Engineering (ASE) reported, in 2019, the FOWLP processes for stacked-patch antennas to enhance the bandwidth [92]. TSMC has reported InFO-based antenna-integrated packages with beamforming capability of antenna array with 6 dBi gain in a 40-nm CMOS RFIC co-designed system [80]. Tsai *et al.* reported an antenna-integrated wafer-level package with a size of $10 \times 10 \times 0.5\,\text{mm}^3$, which shows an antenna-array gain of 14.7 dBi at the 60 GHz band [5]. In addition to the wafer-level packaging, several R&D teams from industry and academic research groups are investigating the potential of fan-out panel-level packaging (FOPLP) with organic substrates or glass substrates [93, 82] for 5G and radar communications.

CHAPTER 3

LOW-LOSS HIGH-DENSITY PACKAGE-LEVEL INTERCONNECTS

High-precision impedance-matched interfaces, low-loss interconnections and feedlines play a significant role in enabling the high performance of antennas and distributed passives in a 5G package. This chapter focuses on the design, fabrication and demonstration of low-loss signal routing for 5G systems. Interconnects in thin glass substrates are described in the first part while those in the multilayered build-up layers with microvia transitions are discussed in the second part.

3.1 Transmission Line in Glass Substrates

3.1.1 Design

This section begins with the design of conductor-backed co-planar waveguides (CB-CPWs) with through-package vias (TPVs) of 30 μm diameter in a 100 μm glass substrate. CPWs, in general, provide lower conductor loss, dispersion, and smaller radiation loss at discontinuities, minimizing crosstalk on the same metallization layer [28, 3]. Moreover, CB-CPWs feature lower-impedance transmission lines and higher structural strength [94]. To characterize the insertion loss per unit length, three types of CB-CPWs with various lengths were modeled and designed. In the designs, a 100 μm glass as a core substrate and TGVs with a diameter of 60 μm were assumed. The configuration, as shown in Figure 3.1a, is determined and optimized with a 3D full-wave EM simulator considering fringing effects, and each dimension is listed in Table 3.1. These CB-CPW structures have a ground line along with the signal line as shown in Figure 3.1a, and the ground lines are connected to TGV arrays with 60 μm diameter so that better ground termination is realized. By placing TGV arrays, less coupling between transmission lines is achieved, leading to higher

isolation from the electromagnetic interference generated by adjacent noise sources such as transmission lines or interconnections.

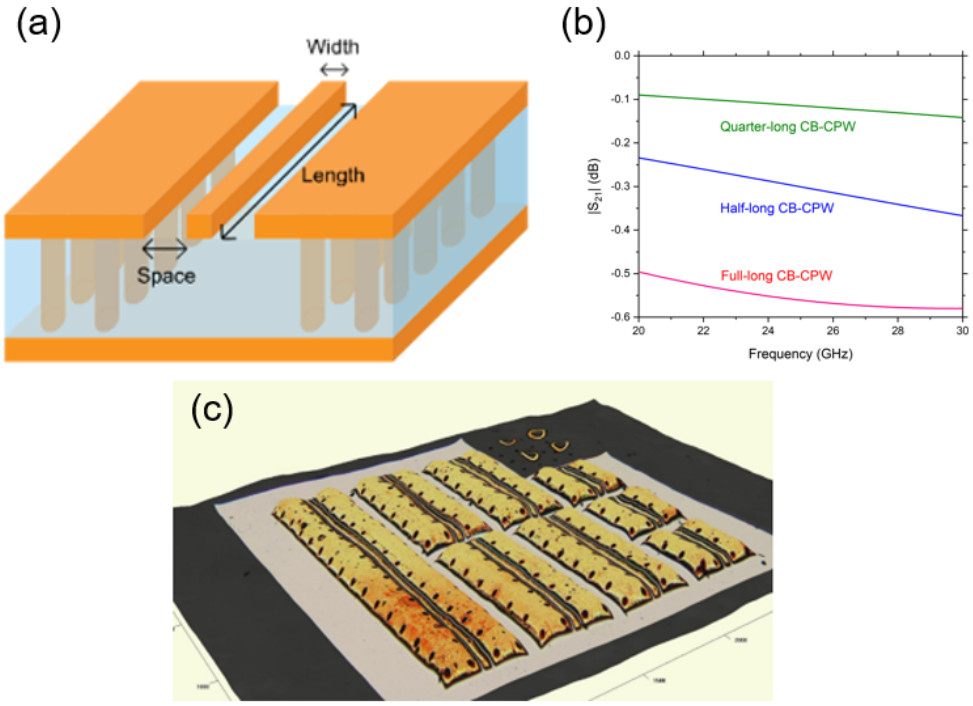

Figure 3.1: (a) Designed CPWG with through-glass vias (b) Simulated insertion losses (c) Fabricated CPWG with different lengths on a glass panel.

Table 3.1: Dimensions of three types of CB-CPW.

Parameters	Width	Space	Length
Quarter-long CB-CPW	181 μm	7 μm	0.42 mm
Half-long CB-CPW			0.90 mm
Full-long CB-CPW			1.86 mm

The EM-simulated frequency responses (i.e., S-parameters), which are generated with HFSS and illustrated in Figure 3.1 (b), show that CB-CPWs over a 100 μm glass substrate results in 0.31 – 0.38 dB/mm. This result is attributed to the dielectric constant (5.0 – 5.4), and loss tangent (0.007), of the glass core. However, the simulations do not take the metal and dielectric surface roughness into account. The roughness at dielectric-conductor interfaces create significant conductor losses that simulations do not detect. From the per-

spective of transmission lines with high precision, tolerance, and low loss, a 100 μm glass core, which enables smooth copper surface, is chosen for this work.

3.1.2 Fabrication

Glass substrates (SGW3 provided by Corning) with prefabricated vias are obtained from Corning Inc. Appropriate handling procedures are required for glass substrate fabrication process in order to address the brittleness and fragility of ultra-thin glass. Polymer lamination on glass is the key to address the challenges with glass handling and metallization of smooth glass surfaces. Low-modulus polymer also acts as a buffer layer that reduces the stress from high CTE copper on glass. Polymer films also enable metallization by acting as an adhesion-promoting layer between electroless copper and glass. In addition, polymer acts as a barrier to prevent copper migration on glass surface between high density wiring under electrical bias.

The glass panels are treated with silane to increase adhesion and prevent delamination during subsequent wet processes. Ajinomoto's GY-11 organic dry films with low dielectric loss of 0.0042 (5.8 GHz) are used in this test vehicle. Polymer lamination was performed with a vacuum laminator, followed by polymer curing. On the laminated polymer, a copper seed layer with a thickness of 0.2 μm is uniformly deposited through electroless plating. Adhesion of electroless copper to polymer is improved by prior roughening of the polymer surface using a permanganate chemical etch to create mechanical anchor sites. The wet chemical etch also cleans the residual polymer that is left on the nearby copper during via drilling processes. Metallization of top and bottom most metal traces and microvias is performed using a semi-additive patterning (SAP) process. Unlike a subtractive patterning, where a thick copper foil is etched off from the undesired areas to form circuit patterns, SAP yields better dimensional and copper sidewall control. This is because SAP avoids the long etching and lateral undercut that is usually prevalent during subtractive etching.

SAP starts with a photolithography step to create micromold patterns of CB-CPWs and

single-patch antennas. A 15-μm dry film UV photoresist that can be patterned with an aqueous developer is employed. Photoresist adhesion strength and the planarity of the substrate can affect the lithography. After the photolithography patterning process, the samples are subjected to 10-minute plasma etching in a chamber filled with O_2 gas to remove photoresist remnants and improve the wettability of copper. Since the thickness of copper is targeted to be 8 μm, the authors strive to obtain 8.2 μm thickness totally, considering the removal of the seed layer at the end of this fabrication process. The photoresist is removed with a stripping solvent, after which the copper seed layer is etched as the last step to obtain the designed mm wave structures. The fabricated structures have a thickness of 8 ± 1 μm over the glass substrates. The fabricated structures of CPWs are shown in Figure 3.1 (c).

3.1.3 Characterization

The electrical performance of the CB-CPWs is characterized by the insertion loss (IL), which represents the magnitude of the transmission coefficient S_{21} in the decibel scale. Three coupons from the quarter-long CB-CPW structure, three coupons from the half-long structure, and two coupons from the full-long CB-CPW are employed for the measurements. Figure 3.2 shows the measurement results of the insertion loss of three types of transmission lines (i.e., quarter-long, half-long, full-long CB-CPWs). Table 3.3 shows the insertion losses at 28 GHz from measurements and compares them with the simulated values.

Table 3.2: Geometry of designed and fabricated CB-CPWs

Name	Width (μm)		Space (μm)		Length (mm)	
	Design	Measured	Design	Measured	Design	Measured
Quarter long	34.1	37.2	7	13.3	0.42	0.417
Half long		38.0		12.7	0.9	0.898
Full long		37.5		13.4	1.86	1.858

As shown in Table 3.3, the measurement results from the eight coupons show agreement with the simulated frequency responses shown in Figures 3.1b and 3.2. Minor discrepan-

cies observed in the half-long and full-long CB-CPWs result from the deviations in the fabricated geometries from the designs. For transmission lines that are shorter in terms of their electrical length, process-related deviations in the geometry of transmission lines do not cause implausible discrepancy. However, for long transmission lines, the deviation in the geometries of the fabricated transmission lines from designed ones (Table 3.2) leads to discrepancy, especially in the 20 – 30 GHz frequency range. One of the key reasons is the electrical wavelength; since the electrical wavelength at 28 GHz in a conductor such as copper is 10.7 mm, the electrical length of the full-long CB-CPWs is almost equivalent to the quarter wavelength. Therefore, in this frequency range, the change in geometries cause disagreement of RLGC parameters used in 3D full-wave simulations, leading to more discrepancy in longer CB-CPWs.

Table 3.3: Measured results of insertion losses of the fabricated CPWGs at 28 GHz

Parameters	Simulations		Measurements	
	IL (dB)	IL (dB/mm)	IL (dB)	IL (dB/mm)
Quarter long	0.131	0.311	0.126	0.274
			0.138	0.301
			0.154	0.334
Half long	0.341	0.355	0.300	0.337
			0.364	0.422
			0.307	0.322
Full long	0.578	0.311	0.544	0.293
			0.567	0.305

3.2 Interconnects in RDLs in Low-Loss Thin Dielectric Films

3.2.1 Design of low-loss transmission lines with microvia transitions

In order to demonstrate superior performance of routing and interconnect layers on thin glass substrates with low-loss dielectric thin-films, six-metal-layer test vehicles with interconnects such as transmission lines and microvia transitions were designed. Transmission-line structures include microstrip lines (Figure 3.3 (a)) and striplines embedded in low-loss dielectric thin-films (Figure 3.3 (b)). In the designs, 50-Ω microstrip-line and stripline

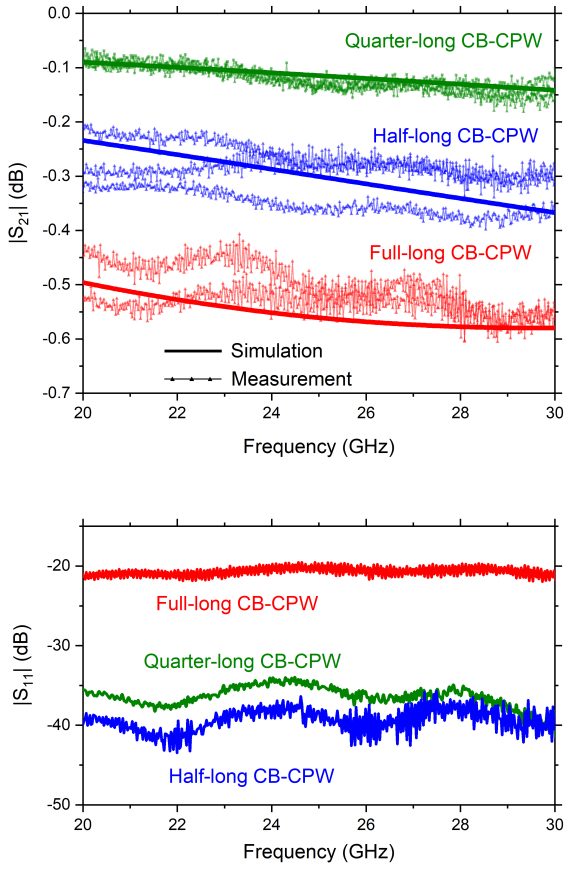

Figure 3.2: Measurement results of the insertion losses (top) and return losses (bottom) of the fabricated CB-CPW.

widths were determined to be 65.6 μm and 6.6 μm from the standing point of impedance matching. Moreover, in order to obtain losses from microvias between the interconnect layers, microvias with a diameter of 40 μm are designed for transitions from a microstrip line to a stripline or vice versa, as shown in Figure 3.3 (c).

Utilizing these interconnect designs, 3D full-wave EM simulations through the HFSS software were performed. Simulations results are illustrated in Figure 3.4. The results indicate that transmission lines provide an average loss of 0.100 dB/mm and that microvias provide an averaged loss of 0.023 dB/microvia both at 28 GHz, calculated from the coupons with microvia transitions, after de-embedding the transmission-line losses.

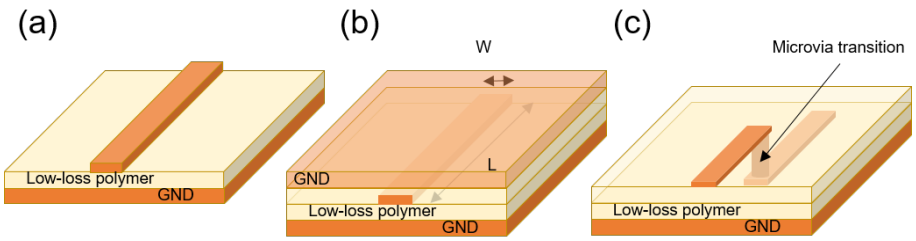

Figure 3.3: 3D view of (a) microstrip lines,(b) striplines, and (c) microvia transitions on low-loss dielectric thin-films.

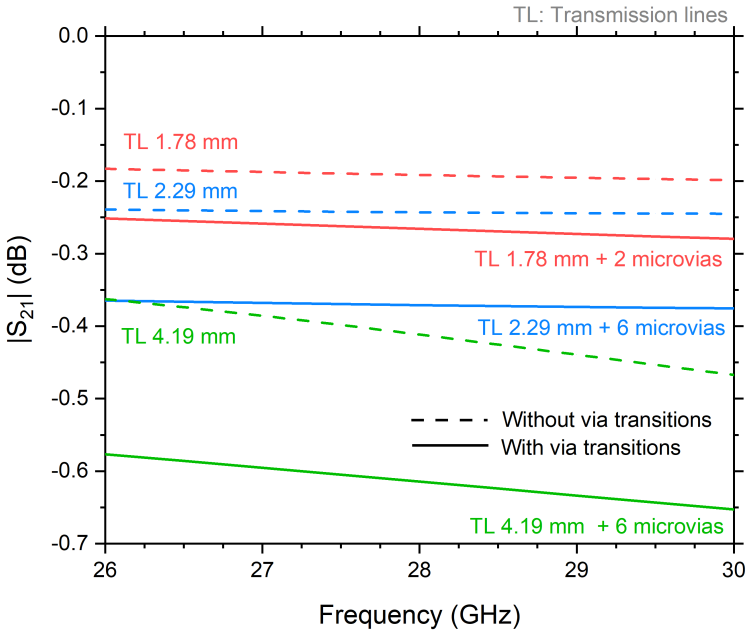

Figure 3.4: Simulation results of transmission-line and microvia losses.

3.2.2 Fabrication of transmission lines and microvia transitions

This section discusses the fabrication of the designed signal-traces on low-loss dielectric thin-films that are laminated onto glass core substrates. The impact of fabrication on electrical performance is also discussed.

In order to fabricate the designed test vehicles with high precision and tolerance, semi-additive patterning (SAP) process is employed. When processed on glass substrates, SAP enables very fine-feature line and space fabrication because of their dimensional stability

and surface planarity. One of the fabricated test vehicles is depicted in Figure 3.5, which includes 50-Ω microstrip lines (Figure 3.5 (b)) and microstrip-stripline transitions with microvias (Figure 3.5 (c)). Cross-sectioning for both side- and front-views was performed to verify the physical dimensions of striplines that have the smallest feature size (6.6 μm) in these test vehicles. The cross-sectioned images are shown in Figures 3.6 and 3.7.

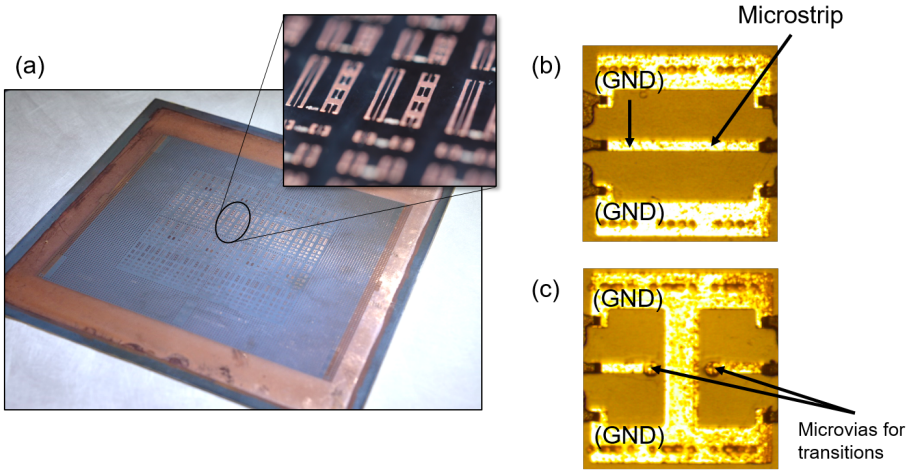

Figure 3.5: Fabricated glass panel with low-loss interconnects, with the inset of a magnified image.

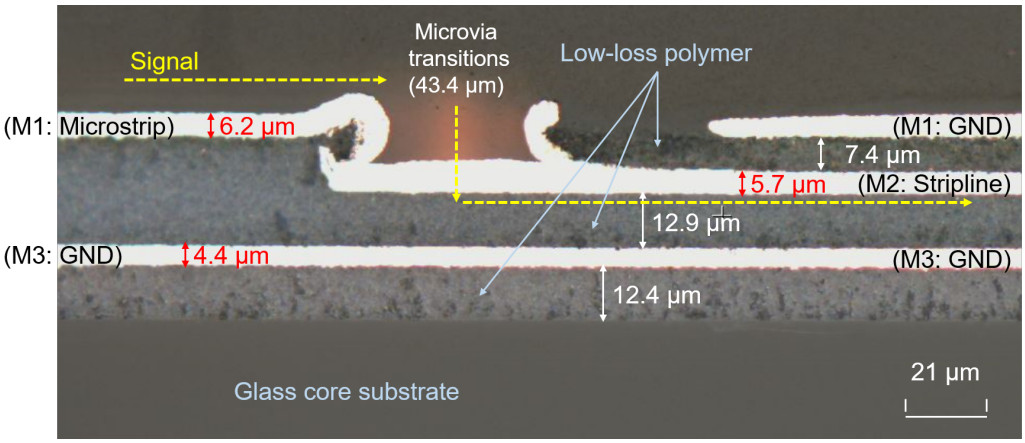

Figure 3.6: Side view of the cross-sectioned transmission liens and microvia transitions designed for the 28 GHz band.

The widths of the fabricated transmission lines were measured through optical microscopy and the measurement results are listed in Table 3.4. The measured widths of

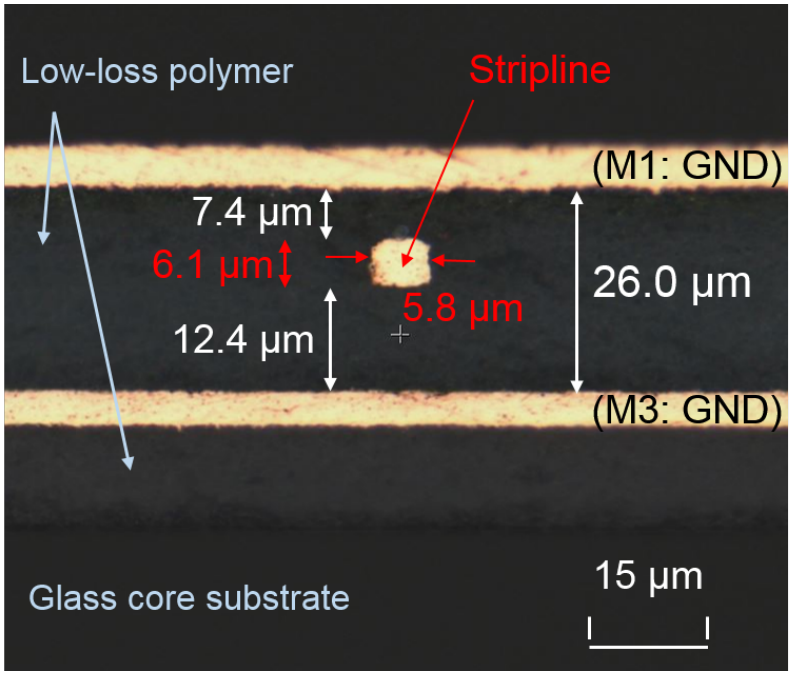

Figure 3.7: Front view of the cross-sectioned stripline designed for the 28 GHz band.

more than twenty coupons for each test vehicle are averaged to remove the dependence on the selected locations across a panel.

While precision of 7-9% with 6-μm striplines was observed, high precision of less than 2% was achieved amongst 65.6-μm microstrip lines. For both the transmission-line structures, the SAP process enabled high precision and tolerance of less than 1.34 μm. Although state-of-the-art high-frequency modules do not entail signal traces or input/output at such small dimensions of a few microns, the next-generation 5G modules are expected to require high precision and control of such low-loss interconnects to enable high-performance IPDs, high routing density, etc.

The thickness of low-loss dielectric thin-films was 12.4–13.0 μm below M2 and M3, while the target is 15 μm, as depicted in Figure 3.6. Similarly, the dielectric film thickness between M1 and M2 was averaged as 7.3 μm, while the target was 7 μm in the designs. Copper thicknesses for RDLs and the ground plane were 5.7–6.5 μm and 4.4 μm, respectively. Although the thickness of the ground plane does not significantly affect the electrical performance, the deviation of RDL thicknesses may change characteristic impedance and,

thus, impedance mismatch that brings about undesired signal reflections and EM radiation that degrades the performance of adjacent components.

Table 3.4: RDL precision fabricated in low-loss polymer laminated on glass substrates

	TV#1	TV#2	TV#1	TV#2
	Microstrip		Stripline	
Target	65.6 μm		6.6 μm	
Measurements	65.13 μm	67.11 μm	6.62 μm	5.60 μm
Variance	0.95 μm	1.34 μm	0.52 μm	0.60 μm
Precision	1.46%	1.99%	7.88%	9.09%

3.2.3 Characterization of Interconnects in RDLs

Electrical characterization of the fabricated low-loss interconnects with transmission lines and microvias were performed in the frequency domain in order to compare the measurement results with simulation results. The data obtained from the measurements were also analyzed.

In order to verify the simulation results, frequency responses of the designed microstrip lines, striplines, microvias, and the combination of them are measured through a two-port vector network analyzer in the frequency range of 26–30 GHz. The results, illustrated in Figure 3.8, show the insertion losses only by transmission lines (Figure 3.8 (a)) and by transmission lines with microvia transitions (Figure 3.8 (b)). Although the overall responses from measurements are consistent with those from simulations, ripples were observed in both of the measurements. This phenomenon is attributed to a certain level of impedance mismatch from 50 Ω that causes wave reflections within the device under test. Impedance mismatch is not caused simply by a change in transmission-line width but also by the deviation of dielectric thickness, conductor thickness, conductor surface roughness and tapered angle of signal traces as observed in the stripline shown in Figure 3.7.

From the frequency responses obtained from each test structure, the losses from transmission lines and microvia transitions are de-embedded, as shown in Figure 3.9. Based on the results, insertion loss per unit length (mm) for transmission lines and that per microvia

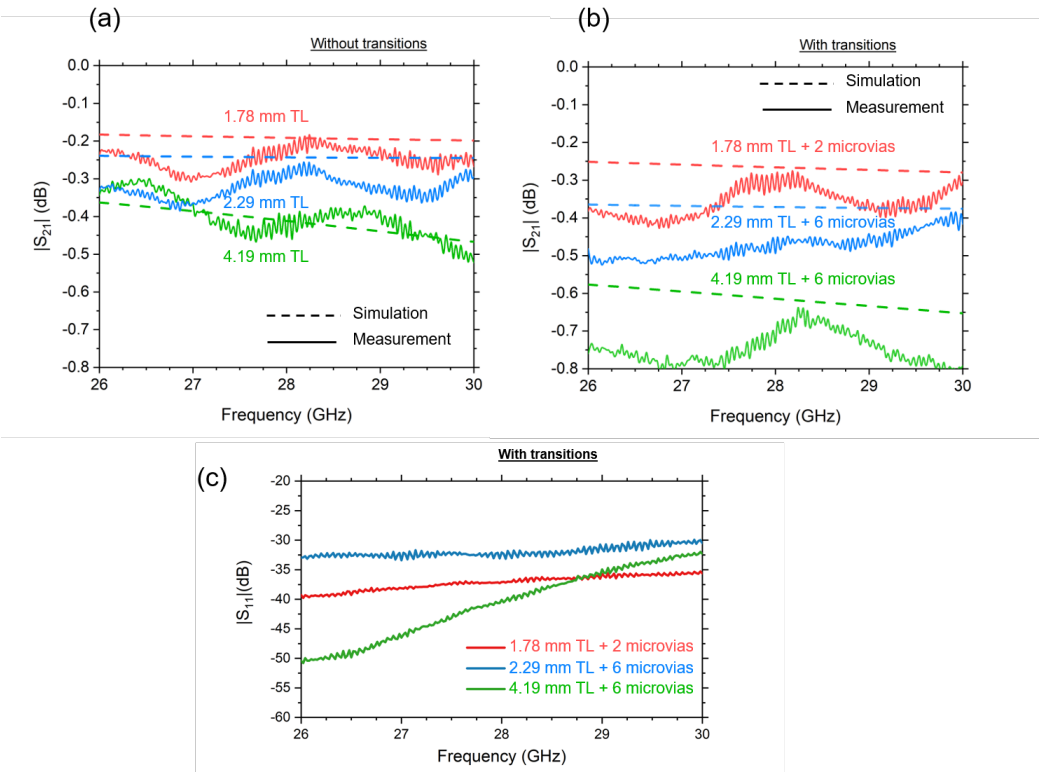

Figure 3.8: Frequency responses of signal interconnects in RDL: (a) $|S_{21}|$ without microvias, (b) $|S_{21}|$ with microvia transitions (c) $|S_{11}|$ with microvia transitions.

are calculated using the linear regression method. Transmission-line losses were measured as 0.103 dB/mm, which is 3% higher than that from the simulations. Although this is mainly caused by the slight impedance mismatch discussed above, this range of deviation does not significantly degrade the performance of a system.

3.3 Ultra-low-Loss Substrate-Integrated Waveguides in Glass-Based Substrates

Ultra-low-loss SIWs fed by co-planar waveguides in thin borosilicate glass and fused silica substrates are investigated forthe 5G New Radio (NR) n257 band (26.5 – 29.5 GHz) for millimeter-wave (mm-wave) applications. This section includes the characterization of the dielectric properties (i.e., relative permittivity, ε_r, and dissipation factor, $\tan\delta$). It also focuses on the designs of SIW based on cut-off frequencies, calibration methodology, and the dimensions of elements. Finally, the insertion losses in borosilicate glass and fused

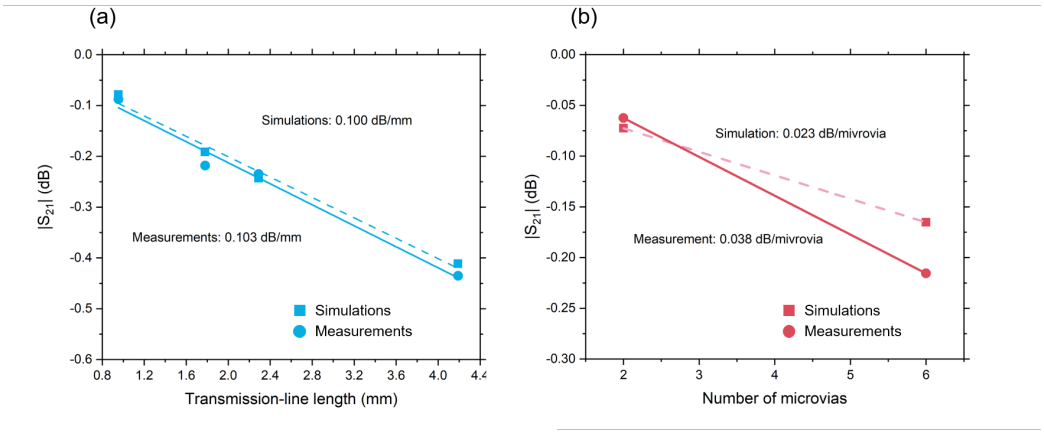

Figure 3.9: Insertion losses of (a) transmission lines and (b) microvias in RDL at 28 GHz.

silica are discussed.

3.3.1 Ring-Resonator Characterization of Fused Silica

To accurately characterize the dielectric properties of fused silica, which is widely used for high-performance optical fibers, ring resonators that characterize relative permittivity, ε_r, and dissipation factor, $\tan\delta$, were designed at 24.6, 27.0, and 29.8 GHz. The ring resonators were fabricated directly on fused silica, as depicted in the inset of Figure 3.10 using the semi-additive patterning (SAP) process. The measured return loss and insertion loss of the ring resonators designed for the three frequencies are plotted in Figure 3.10. From the resonant frequencies and the 3-dB bandwidths, relative permittivity and dissipation factor were derived [95, 96]. The dielectric properties are calculated from the dielectric loss and conductor loss based on surface roughness and metal conductivity. The derived results are listed in Table 3.5, showing approximately ten times lower dissipation factors than other low-loss organic dielectric materials used for 5G/mm-wave applications. This result from the ring-resonator characterization using a thin substrate is consistent with the reported dielectric properties of bulk fused silica [46].

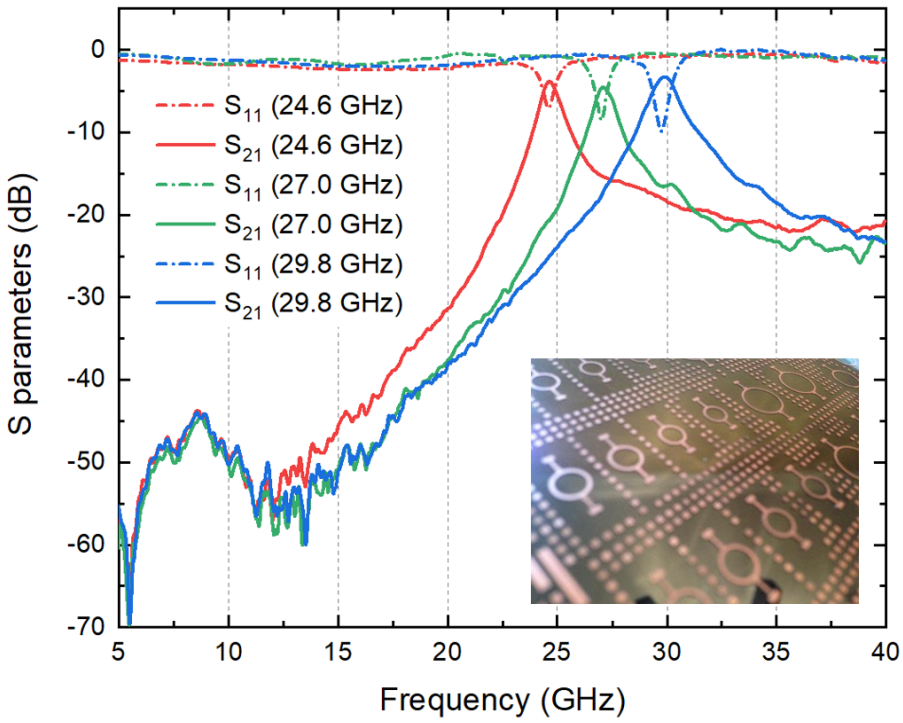

Figure 3.10: Measured frequency responses for ring resonators designed at three frequencies with an inset figure of the fabricated test vehicle.

Table 3.5: Measured Dielectric Properties of Fused Silica

	25 GHz	27 GH	30 GHz
Dielectric constant, ε_r	3.85	3.78	3.74
Dissipation factor, tan$\delta(\times 10^{-4})$	3.29	3.26	3.83

3.3.2 Modeling and Design of Substrate Integrated Waveguides

Based on the characterized dielectric properties, we designed the conductor-backed coplanar waveguide (CPWG)-fed SIWs for borosilicate glass and fused-silica substrates laminated with 15-μm low-loss dielectric films, as depicted in Figures 3.11 (a) and (b). To de-embed the insertion loss of CPWG, T(through)-R(reflect)-L(line) structures were also designed, as shown in Figures 3.11 (c)–(e). The detailed simulations were performed using an electromagnetic finite-element method solver, HFSS. The SIW consists of two metal planes and two arrays on through-glass vias (TGVs) to form a rectangular parallelepiped. In the waveguide, only the TE_{10} (TE: transverse electric) mode propagates in the waveguide,

while the TE_{20} mode is cut off in the target frequency range, 24–42 GHz, as shown in Figure 3.12. Equation 3.1 indicates that the selection of TE_{n0} modes allows to design ultra-thin waveguides in packaging substrates. While the length of SIWs l_{SIW} is 4 mm, the thicknesses of borosilicate glass and fused silica are 100 μm and 210 μm, respectively.

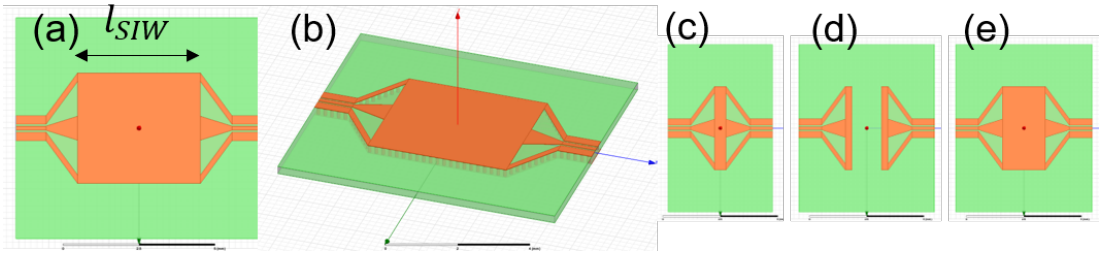

Figure 3.11: SIW designs in HFSS with (a) top view with a length, l_{SIW}, of 4 mm and widths of 3.08 mm and 3.68 mm for borosilicate glass and fused-silica glass, respectively (b) 3D view and high-accuracy precision method with (c) through, (d) reflect, (e) line.

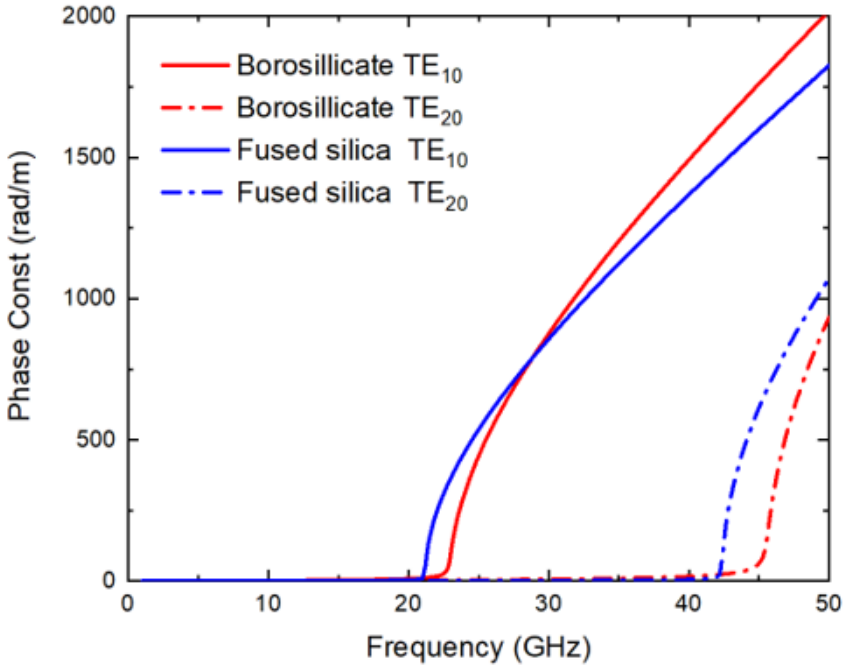

Figure 3.12: Cut-off frequency of the TE_{10} and TE_{20} modes for borosilicate glass and fused silica.

$$f_{\text{c,mn}} = \frac{1}{2\pi\sqrt{\mu\epsilon}}\sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{h}\right)^2} \tag{3.1}$$

3.3.3 Fabrication of SIWs in borosilicate glass and fused silica

To verify the designed models, the SIWs are fabricated through SAP process as illustrated in Figure 3.13. The lamination of thin low-loss polymer with a relative dielectric constant of 3.3 and a dissipation factor of 0.0044 on glass substrates enhances the adhesion strength of copper to the substrate and mitigates the residual stress between the core substrate and copper patterns and thus prevents copper traces from delaminating from the substrate. This patterning process enables high tolerance below 2 μm on glass-based substrates, which minimize the impedance deviation from designs and thus achieve high model-to-hardware correlation Figure 3.14.

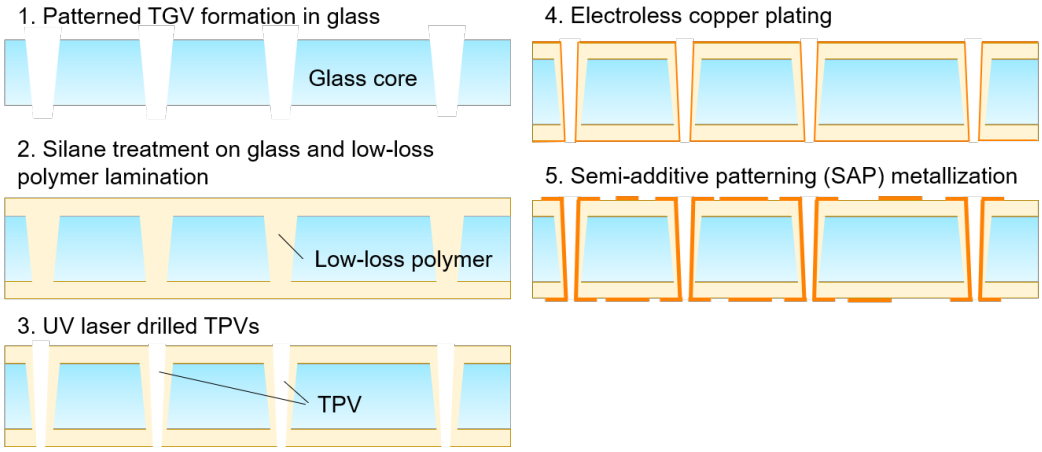

Figure 3.13: Process flow for semi-additive copper patterning [51] on glass core laminated with thin low-loss dielectric polymer films.

3.3.4 Characterization Results and Analysis

Table 3.6: Comparison of the de-embedded insertion losses between simulations and measurements.

	Borosilicate glass		Fused silica	
	dB	dB/mm	dB	dB/mm
Simulation	-0.552	-0.138	-0.092	-0.023
Measurement	-0.484	-0.121	-0.071	-0.018

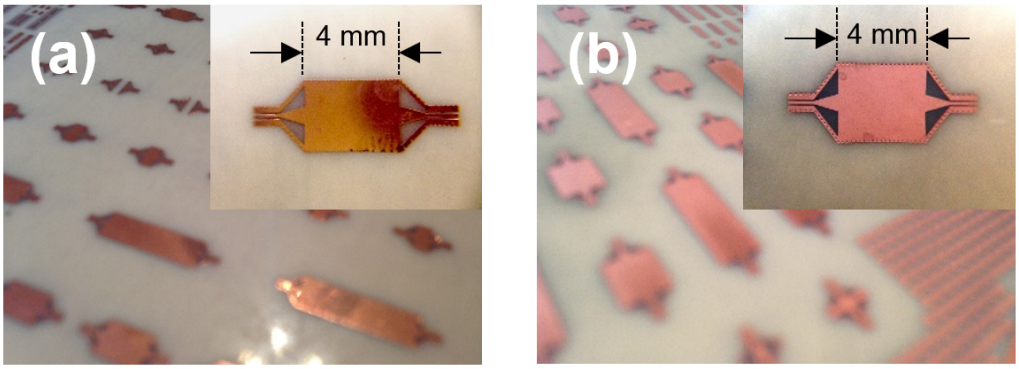

Figure 3.14: Fabricated SIWs with TRL calibration structures in (a) borosilicate glass and (b) fused-silica substrates.

This section discusses the characterization results of the fabricated SIWs. The measurements are performed through a vector network analyzer and a pair of GSG probes that are accurately calibrated up to 40 GHz. Figure 3.15 shows the intended cut-off frequency at around 24 GHz and excellent correlation between simulations and measurements of CPWG-fed SIWs for both borosilicate glass and fused silica. To obtain precise insertion losses at the target frequency, 28 GHz, the vector network analyzer was re-calibrated in a narrow frequency range. The measured frequency responses are plotted in Figure 3.16 along with their averages and standard deviations computed from eight samples in each substrate.

Based on the SIW results and measured TRL structures, the insertion losses of SIW were de-embedded from CPWG and the transition between CPWG and SIW. The de-embedded results are listed in Table 3.6, showing an insertion loss below 0.02 dB/mm with the fused silica substrate.

The comparison of insertion losses of SIWs with various low-loss substrates is listed in Table 3.7. While the thickness reduction of substrates causes an increase in insertion losses, the comparison indicates that borosilicate glass has the potential to reduce thickness. The fused-silica substrates achieve 0.018 dB/mm, which is 2X reduction in insertion loss compared to that of the organic-based SIWs. This low-loss SIW in fused silica is pre-

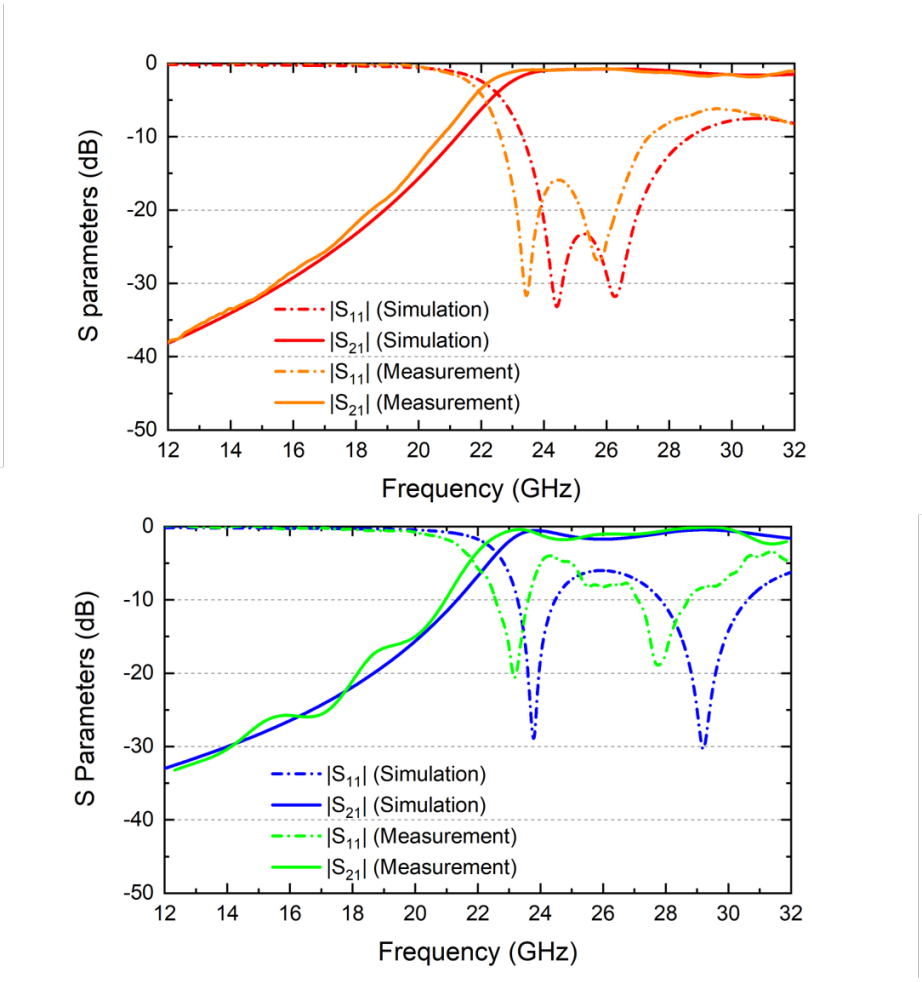

Figure 3.15: Simulated and measured results of fabricated SIWs with CPWG and the transition between them.

dominantly enabled by its low dissipation factor. In addition, the stack-up of a fused-silica core laminated with 15-μm low-loss dielectric films offer higher adhesion, lower interfacial stress, and higher reliability than metallization directly on a fused-silica glass core [46].

3.4 Low-loss Impedance-Matched Sub-25-Micron Vias

3.4.1 Design – Microvia impedance matching

In addition to the geometrical seamless transition between transmission lines and microvias, control of microvia impedance is critical to lower the return loss and maximize the power transfer. We model a representative microvia and adjacent ground vias, as illustrated

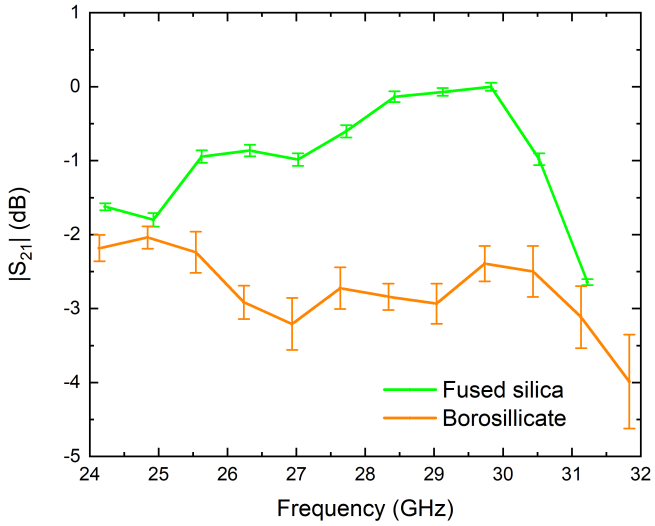

Figure 3.16: Measured results focusing on the 28-GHz frequency band.

in Figure 3.17 (a). Similar to transmission-line and TPV models, we defined an equivalent circuit illustrated in Figure 3.17, called the LRCG model [97, 98]. This section targets the microvia diameter below 40 μm, while through-package vias are studied with larger diameters (>100 μm) [68, 69, 99, 100]. The impedance in the equivalent circuit consists of the resistance (R), conductance (G), and inductive (L) and capacitive (C) reactance as described in Figure 3.18 and Equations 3.2 – 3.9.

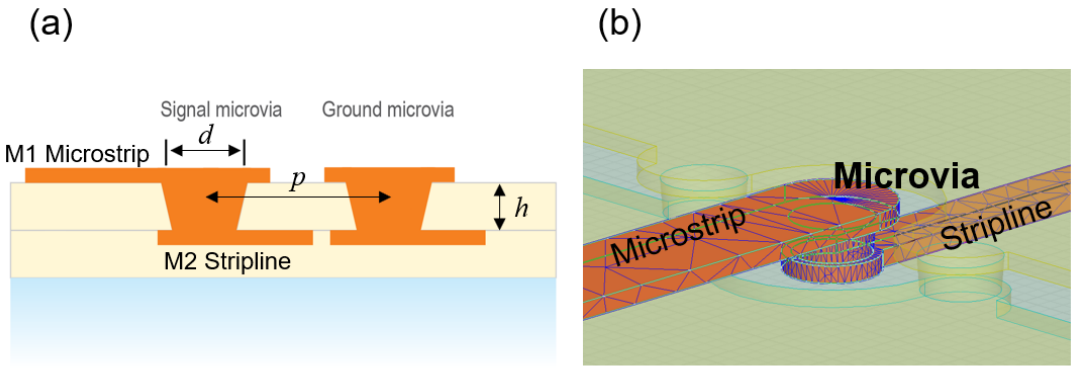

Figure 3.17: Modeled microvia for the signal and ground paths. (a) a cross-section view with dimensions (b) a 3-D view for FEM simulations.

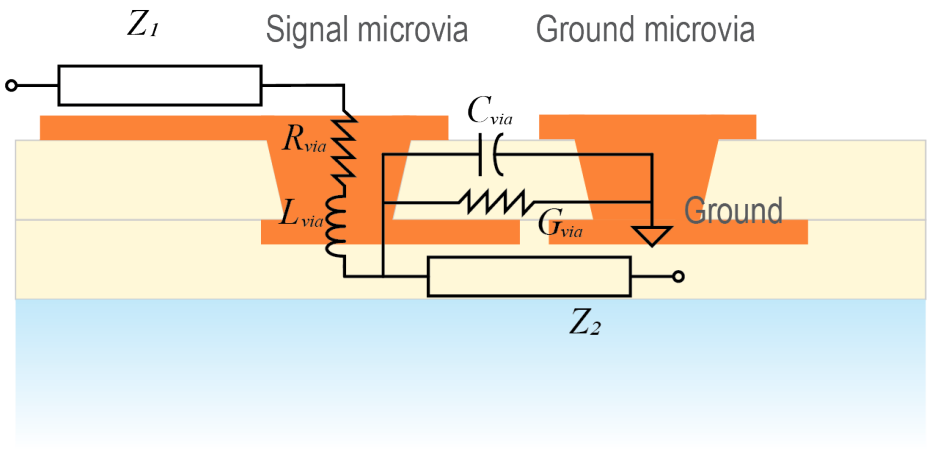

Figure 3.18: LRCG equivalent circuit for microvias surrounded by transmission lines (Z_1 and Z_2).

The resistance per unit length of a microvia, R_{via}, comprises the direct-current (DC), $R_{\text{via,dc}}$, and alternative-current (AC) resistances, $R_{\text{via,ac}}$. In the frequency range where $R_{\text{via,dc}}$ is dominant, the via resistance is equal to the DC resistance. However, once the skin depth becomes more dominant, the via resistance is given by the AC resistance. Overall, the via resistance is given as

$$R_{\text{via}} = \begin{cases} R_{\text{via,dc}} & (r \leq \delta_{\text{s}}) \\ R_{\text{via,ac}} & (r > \delta_{\text{s}}). \end{cases} \tag{3.2}$$

The DC resistance per unit length, $R_{\text{via,dc}}$, is described by the resistivity of the conductive material (i.e., copper), ρ_{Cu}, and the radius of the microvia, r, as

$$R_{\text{via,dc}} = \rho_{\text{Cu}} \frac{1}{\pi r^2}. \tag{3.3}$$

In contrast, the AC resistance, $R_{\text{via,ac}}$, is a function of frequency that is incorporated in the skin depth, δ_{s}, and is written as

$$R_{\text{via,ac}} = \frac{p}{2r} \rho_{\text{Cu}} \frac{1}{2\pi r \delta_{\text{s}}}, \tag{3.4}$$

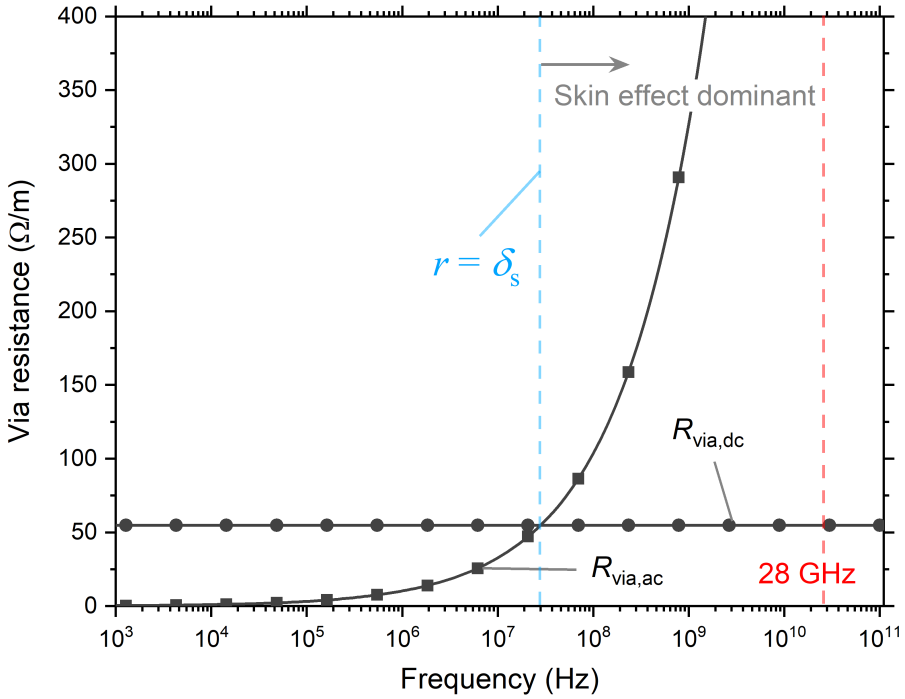

Figure 3.19: Frequency dependence of via resistance, R_{via}, with a microvia diameter of 20 μm.

where the approximation, $r\delta_s \gg \delta_s^2$, is applied. The $\frac{p}{r}$ denotes the proximity factor [101]. Equation 3.4 and Figure 3.19 imply that $R_{\text{via,ac}}$ increases with the increasing frequency. The overall resistance, R_{via}, is dependent on the skin effect in the frequency range of interest, as depicted in Figure 3.19.

The parasitic inductance, L_{via}, caused by the microvia is modeled similarly to the inductance of a wire lying in a direction and is given by

$$L_{\text{via}} = k\frac{\mu_{\text{Cu}}}{2\pi}\ln\left(\frac{p}{r}\right), \tag{3.5}$$

where the permeability of copper, μ_{Cu}, is approximated to the one in the vacuum in the model.

The parasitic capacitance, C_{via}, between the signal and ground vias depends on the

relative permittivity of the dielectric, ε_{r}, and is expressed as follows:

$$C_{\text{via}} = \frac{1}{k}\frac{\pi\varepsilon_{\mathrm{r}}\varepsilon_0}{\ln\left(\frac{p}{r}\right)}, \tag{3.6}$$

where ε_0 denotes the vacuum permittivity. A scale factor, k, is essential to correlate the LRCG and FEM models. The scale factor for the inductance and capacitance explains the difference in the geometrical assumption. The LRCG model assumed continuously-surrounding ground vias around the signal via, while the FEM simulation employed two adjacent ground vias as depicted in Figure 3.17 (b) with a pitch, p, of 50 μm.

The conductance, G_{via}, is described as

$$G_{\text{via}} = \frac{\sigma_{\text{poly}}}{\varepsilon_{\mathrm{r}}\varepsilon_0}C_{\text{via}}, \tag{3.7}$$

and also attributed to the dielectric property of between the vias and the conductivity of the polymer, σ_{poly}, which is followed by

$$\sigma_{\text{poly}} = 2\pi f\varepsilon_{\mathrm{r}}\tan\delta. \tag{3.8}$$

The conductance of microvias is nearly negligible in Equation 3.9 because of the low loss tangent (tanδ) and low C_{via}. This equation is applicable below the breakdown voltage of the dielectric.

Derived from Equations 3.2 – 3.8, the microvia impedance, Z_{via}, is summarized as

$$Z_{\text{via}} = \sqrt{\frac{R_{\text{via}} + j\omega L_{\text{via}}}{G_{\text{via}} + j\omega C_{\text{via}}}}, \tag{3.9}$$

where ω denotes the angular frequency, which is also given as $2\pi f$.

Using Equations 3.2 – 3.9, we computed all the electrical characteristics based on the parameters summarized in Table 3.8. The low microvia diameters provide the potential to enable high-density packaging for RF/mm-wave applications. The computed result based

on the LRCG model is plotted in Figure 3.20.

To verify the LRCG model, the FEM-based simulation was also conducted through a 3D electromagnetic-wave solver, as depicted in Figure 3.17 (b). The FEM-based simulation accuracy highly correlates with the mesh size; to capture the effect of microvias in FEM accurately, mesh sizes smaller than the skin depth at 28 GHz were defined in microvias during the simulation.

The results shown in Figure 3.20 indicate that the microvia characteristic impedance increases with the decreasing diameter. The main attributes of the increase are the AC resistance, $R_{\text{via,ac}}$, inductance, L_{via}, and capacitance, C_{via}.

It is noted that the increase in microvia characteristic impedance degrades the signal-noise ratio in the digital domain; however, in the analog domain such as RF signal routing, it is significant to make each element to be close to 50-Ω impedance in complicated RF systems to minimize the refection loss or voltage standing wave ratio (VSWR). The minimized reflection loss and VSWR lead to maximum power transfer and normal functioning of RF elements.

Based on the parameters listed in Table 3.8, the insertion loss of daisy chains, S_{21}, was simulated at 28 GHz in the 3D full-wave solver. The daisy chains consist of 50-Ω microstrip lines, 50-Ω asymmetric striplines, and microvias with various diameters ranging from 20 to 35 μm. The daisy chains are designed so that only microvia impedance affects the entire impedance while the impedance of transmission lines remains 50 Ω. The frequency response is plotted in Figure 3.21.

3.4.2 Processes for Forming Small Microvia

Diameter control and surface flatness of microvias

Microvia is defined as a via with a diameter below 150 μm. In addition to mechanical drilling, three techniques are widely used to form microvias in printed circuit boards (PCB) [102] and packaging substrates and build-up layers [103]: plasma etching, photo-

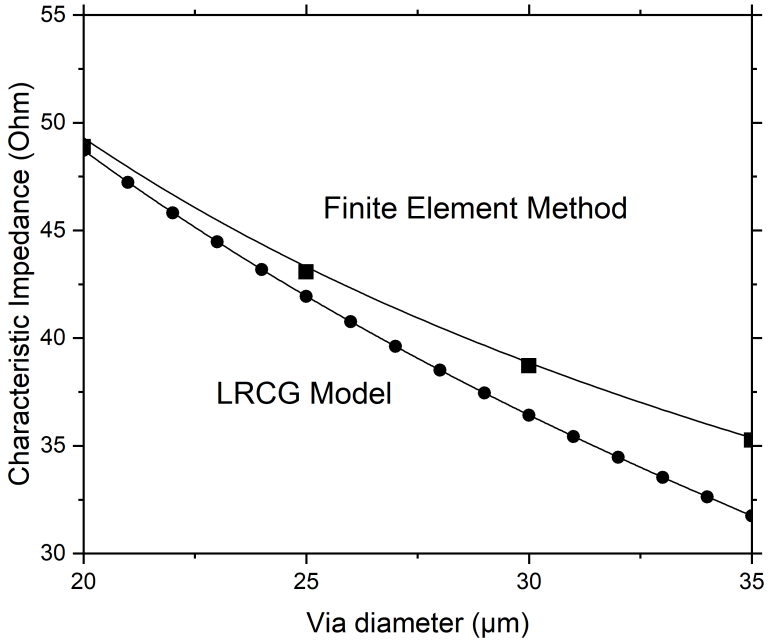

Figure 3.20: Characteristic impedance of the microvia derived from the LRCG and FEM models as a function of the microvia diameter.

lithography, and ultraviolet (UV)-laser ablation. Plasma etching faces several challenges in achieving small feature size with high yield, particularly in dielectrics with high filler content. It also requires several process steps. Photo-lithographic microvia formation technique utilizes photosensitive dielectric, applies UV exposure, and patterns microvias concurrently [104]. This technique is capable of achieving a diameter of 2 – 3 μm and primarily used for high-density interconnect substrates [105, 106]. This technique, however, is limited by the availability of photosensitive dielectric materials.

UV-laser ablation has been the mainstream for two decades in build-up layers. CO_2 laser generates heat and decompose the dielectric material to form microvias, and the microvia diameter is limited up to 40 μm because of the thermal effect and the wavelength of the beam around 10 μm. The excimer laser technique is employed for the semiconductor industry due to the relative-short wavelength (126 nm – 351 nm) with the ability to form sub-5 μm microvias [107]. This technique still remains challenging because of the

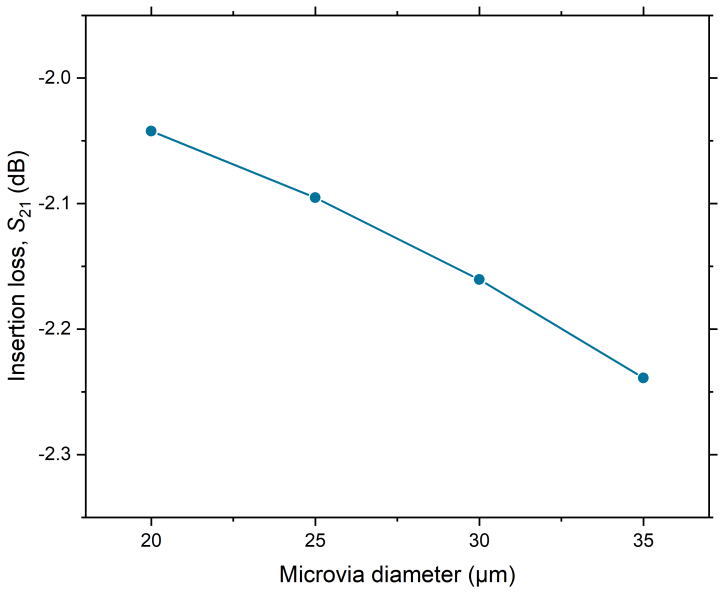

Figure 3.21: Insertion loss of microvias at 28 GHz with various microvia diameters.

cost. UV laser ablation using the third harmonic of the original wavelength of 1,064 nm generates a coherent beam with a wavelength of 355 nm to drill microvias in dielectric. This method, employed in this study, is scalable to high throughput at low-cost [108, 109] and is also capable of controlling microvia diameters to below 8 μm [106]. Comparing the micromachining quality and the cost of UV lasers with pulsewidths of nanosecond, picosecond, and femtosecond, R. Patel *et al.* reported that picosecond and femtosecond laser are preferred for high-throughput and high-quality micromachining at lower cost per watt [110]. The microvia-drilling tool from Electro Scientific Industries, Inc. is equipped with a coherent solid-state laser that yields picosecond pulses at a repetition rate of 80 MHz, which leads to high throughput of microvia fabrication and has the ability to form over 10 thousand vias per second during operation.

Compared to UV laser with a nanosecond pulse, picosecond pulse utilized in this study yields less heat in a dielectric and thus facilitates the control of microvia diameter. Microvias with different diameters are formed by the spiral raster mode, where the 355-nm UV beam moves outward from the center to a large turn in a spiral motion. The optimiza-

tion was performed to obtain the targeted microvia diameters with the parameters: a pulse power of 0.5 W, a circumferential pitch of 1 μm, a radial pitch of 1 μm, and a number of turns (10, 8, 6, 4) for diameters of 35, 30, 25, and 20 μm, respectively. The spiral-raster drilling is executed four times consecutively to ablate and remove the polymer. The drilled microvias with copper filled are shown in Figure 3.24.

Multi-layer fabrication process

The designed microvias with transmission lines were fabricated through the semi-additive patterning (SAP) process and the picosecond UV laser tool. The overall fabrication process is illustrated in Figure 3.22. The surface was cleaned by bombarding Argon for 30 minutes with a power of 150 W to remove residue after microvia drilling.

The test vehicle employed a liquid dielectric with no fillers in order to minimize the surface roughness on the microvias. As shown in Figure 3.23, the side-wall of the 20-μm-diameter microvia has a smooth surface. The dielectric material [54] provided by JSR Corporation offers good process control of the width of transmission-lines, dielectric thickness, smooth surface, and adhesion to copper without delamination, as depicted in Figure 3.24 (e). The microvia-drilling tool from Electro Scientific Industries, Inc. also provided good control of microvia diameters, as shown in Figure 3.24 (a)–(d). The diameter varies from 20 μm to 35 μm with a step of 5 μm. The microvia-ablation tool used in this work is a UV laser system, which is equipped with a coherent solid-state laser that generates picosecond pulses at a repetition rate of 80 MHz.

3.4.3 Electrical Characterization and Analysis of GCPW on Glass

The test vehicle consists of the daisy chains (i.e., 50-Ω microstrip lines, 50-Ω striplines, and microvias with various diameters ranging from 20 μm to 35 μm with a step of 5 μm). The height of the microvia diameters is identical to the thickness of the dielectric layer, which is 15 μm. The test vehicle included six microvias in a chain to quantify the charac-

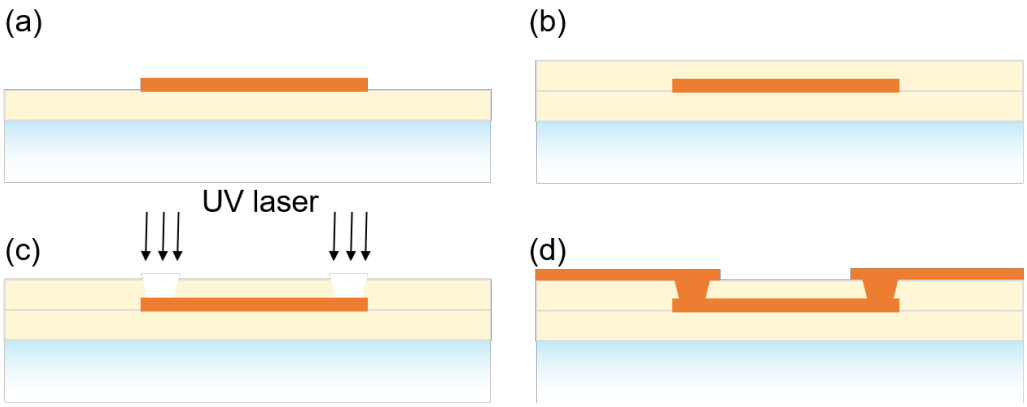

Figure 3.22: Process flow of microvias formed in dielectric layers. (a) SAP process on a dielectric layer (b) Spin coating of the liquid-type dielectric material (c) Microvia drilling using a UV laser tool (d) SAP process with microvias filled with copper.

teristics of microvias with different diameters. A part of the test vehicle is shown in Figure 3.24 (e).

The fabricated test vehicles with transmission lines and microvias are characterized at 28 GHz utilizing a vector network analyzer with the 50-Ω system. The characterization results are shown in Figure 3.25. To quantify the effect of microvias, the dimensions of microstrip lines and striplines were kept the same in the fabricated test vehicle, while changing the microvia diameter and microvia pad size. The diameter of microvia pads were designed to be 5 μm larger than the microvia diameter to mitigate the impedance discontinuity at the pads.

The characterization results indicate that the input impedance of the entire daisy chain with microvias and transmission lines increases with the smaller microvia diameters and becomes closer to 50 Ω. The input impedance is derived from the return loss of the chains. The result is consistent with the trend of the LRCG and FEM models. The minimal discrepancy between the models and the measurements results from the deviation of microvia diameters, the taper angles, and slight thickness variation of dielectric layers.

The daisy chain with 34.2-μm microvias showed an input impedance of 46.6 Ω, which led to an insertion loss of -2.4 dB throughout the chain. In contrast, the chain with 19.8-μm microvias achieved 49.2 Ω, resulting in an insertion loss of -2.18 dB. The change

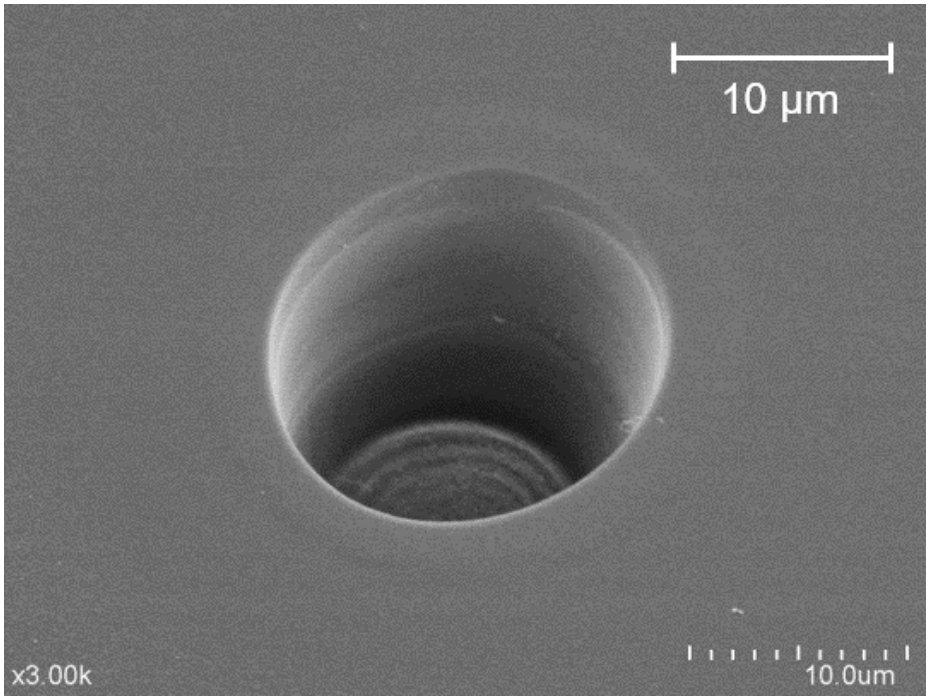

Figure 3.23: SEM image of a microvia with 20-μm diameter.

in microvia diameter without changing the transmission line geometries brought higher impedance matching in the daisy chains and resulted in a 10% reduction in insertion losses caused by microvias. The discrepancy between simulations and measurements in input impedance could be attributed to the variance of the dielectric constant of the dielectric material. The higher insertion loss in measurements than in simulations can be explained by the factors that are not assumed in simulations such as probe-to-pad parasitics or higher radiation from transmission lines due to the roughness of copper patterns. The trends are, however, observed to be consistent between simulations and measurements, as shown Figure 3.25.

It is found that small microvias with a diameter below 30 μm not only lead to high-density signal routing and power distribution in the front-end packages, but also enable seamless impedance matching from one transmission line to another (e.g., a microstrip line to strip line) in mm-wave bands. The need for high-bandwidth computing with heterogeneous integration is advancing fine-pitch RDLs and processes with microvias approaching

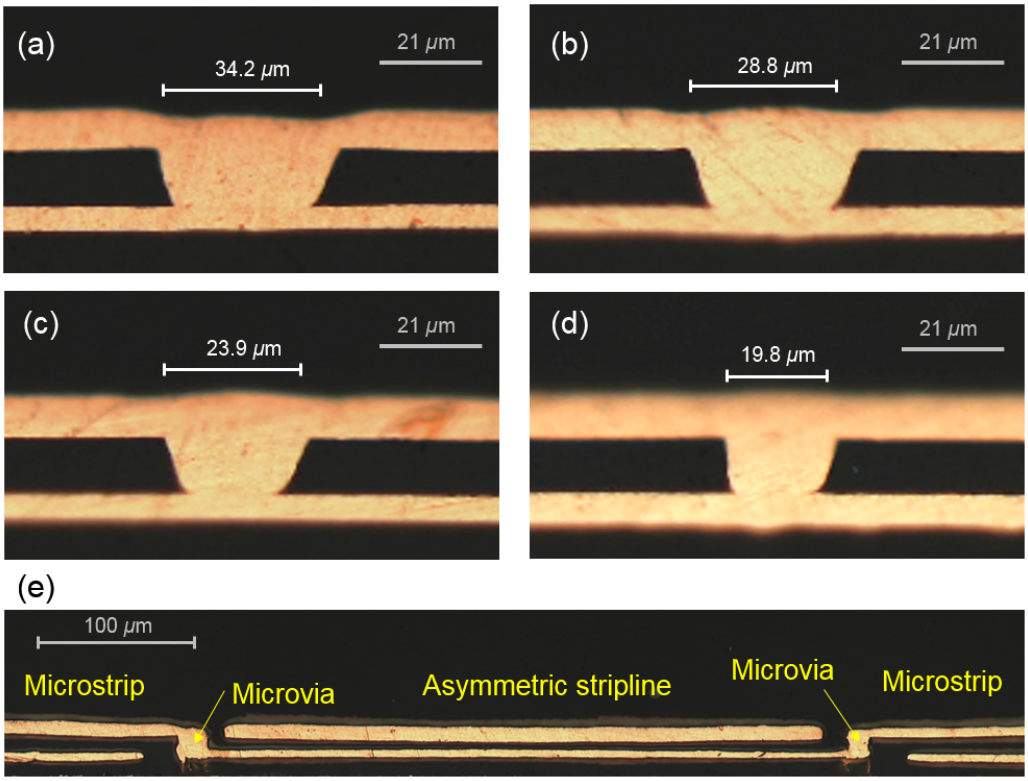

Figure 3.24: Cross-section microscope images with various microvia diameters (a)–(d). The diameters are measured at the center of the tapered microvias. A part of the fabricated daisy-chain test vehicles with transitions from transmission lines to 20-μm microvias (e).

less than 8 μm. The demand for miniaturization and high-performance of 5G mm-wave systems also drives the advancements in highly-precise sub-30-μm transmission lines and microvias.

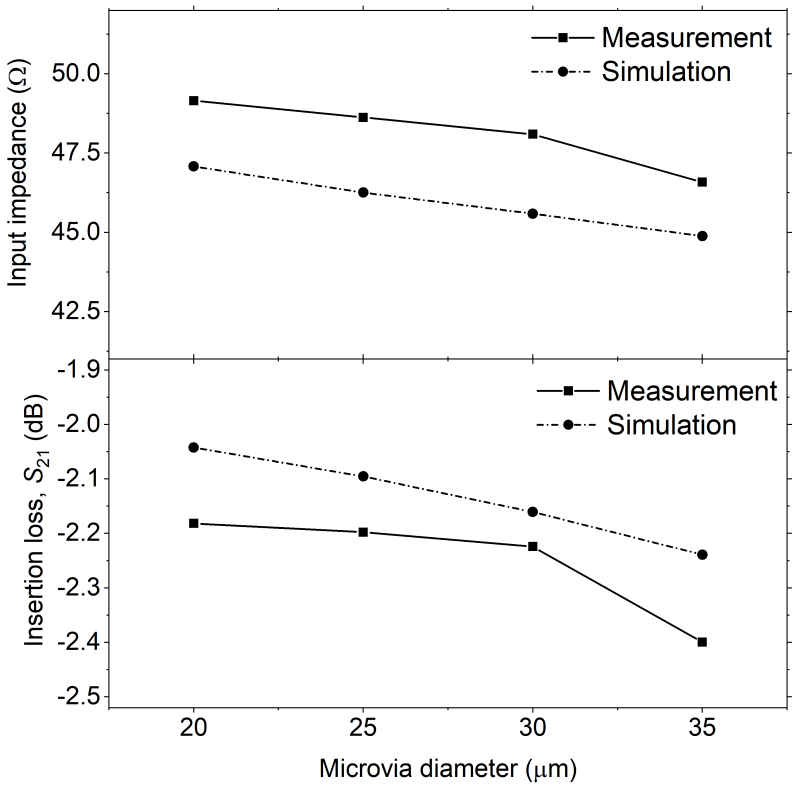

Figure 3.25: Measured input impedance and insertion losses at 28 GHz within the daisy chain of microvias and transmission lines with various microvia diameters.

Table 3.7: Comparison of the insertion loss of SIW with various packaging substrates.

	[70]	[71]	[72]	[73]	This work	This work
Material	LCP	Hydrocarbon ceramic	PTFE	PTFE	Borosilicate glass	Fused silica
Dielectric constant, ε_r	3.16	3.38	2.2	2.94	5.4	3.78
Dissipation factor, tanδ	0.0049	0.0027	0.0009	0.0012	0.006	0.0003
CTE (ppm/K)	17	40	125	12	3.8	0.6
Thickness (μm)	127	1524	254	508	100	210
Frequency (GHz)	50–70	7–14	50–75	50–75	24–40	24–40
Insertion loss (dB/mm)	0.12	0.038	0.042	0.035	0.121	0.018

Table 3.8: Microvia metrics utilized in the calculation of the microvia impedance.

Parameter	Description	Value
f	Operating frequency	28 GHz
d	Microvia diameter	20–35 μm
h	Microvia height	15 μm
p	Microvia pitch	50 μm
k	Scale factor	1.15
ε_r	Relative permittivity of polymer	2.6
$\tan\delta$	Dissipation factor of polymer	0.005
ρ_{cu}	Resistivity of copper	$1.7 \times 10^{-8}\Omega$·m
δ_{s}	Skin depth	0.39 μm at 28 GHz

CHAPTER 4
DESIGN AND DEMONSTRATION OF GLASS-BASED ANTENNA-INTEGRATED MM-WAVE MODULE PACKAGES

This chapter discusses the design and demonstration of antenna-integrated glass-based packages for 28-GHz bands. The first part (Section 4.1) of the chapter focuses on the *chip-last* or flip-chip-assembly antenna module with package-level design for antenna-integration, package miniaturization, process development for low-loss interconnects with through glass vias, and the characterization of key building blocks: 1) co-planar waveguides and TPVs, 2) dipole Yagi-Uda antenna, and 3) flip-chip assembled LNA with 80-μm solder balls. The second part (Section 4.2) of this chapter presents the *chip-first* or glass-panel embedding (GPE) approach for antenna integration. This section also begins with the process development, followed by the integration of band-selection filters and dual-polarized patch antenna arrays while quantifying the benefits of the GPE architecture for AiP applications.

4.1 Ultra-Thin Antenna-Integrated Glass-Based mm-Wave Package

This section presents the design and demonstration of a high-bandwidth AiP module focusing on low-loss interconnects from chip to antenna with a 100-μm-thick low-CTE glass, in the 5G mm-wave frequency bands (i.e., n257, n258, n261). Section 4.1.1 introduces the stack-up of the package and key design rules to miniaturize the antenna-integrated package with low-loss interconnects that are matched to the designed system impedance. While the development of re-distribution layers (RDL) on glass is discussed in [23], Section 4.1.2 focuses on the via-in-via vertical interconnects and fine-pitch IC assembly that are critical to obtain desired electrical performance of package-integrated antennas and active ICs. In addition to the fundamental characterization of transmission lines performed in [8], Sec-

tion 4.1.3 describes the detailed characterization of low-loss chip-to-antenna interconnects with transmission lines and through-package vias (TPV) in the wider frequency band, high-bandwidth Yagi-Uda antennas, and IC assembly on the fabricated glass substrates. Along with the comparison of the proposed work with recent leading-edge reports (Section 4.1.4), the conclusions are compiled in Section 4.1.5.

4.1.1 Design of the Stack-up of the Antenna-Integrated Glass-Based mm-wave Package

This section discusses the design of the four metal-layered-RDL mm-wave module including the antenna patterning, die assembly, signal routing, and power distribution. The stack up is shown in Table 4.1. The module design begins with the antenna selection and placement. A well-known dipole Yagi-Uda antenna with one director and a balun is designed and implemented on the top metal layer (M1) in the test vehicle to meet the bandwidth that covers 24.25 – 29.5 GHz. Yagi-Uda antennas feature a main lobe in the azimuth plane with a single polarization, while the most radiation of patch antennas directs in the vertical plane. The selection of antennas depends on the application of the modules to be implemented. The main advantages of the dipole Yagi-Uda antennas are the design simplicity, wide bandwidth, and control of the gain of the main lobe by changing the number of directors.

Table 4.1: Stack-up of the four metal-layered glass-based antenna module.

M1	Antenna patterns, feedlines, transmission lines
15-μm build-up polymer	
M2	Partial ground plane
15-μm build-up polymer	
100-μm glass core	
15-μm build-up polymer	
M3	Partial ground plane
15-μm build-up polymer	
M4	Transmission lines, bump pads, power plane

In this test vehicle, the dipole Yagi-Uda antenna is fed by a microstrip line transitioned from a conductor-backed co-planar waveguide (GCPW). CPW or GCPW signal routing

is more common for multi-layered package than microstrip lines or striplines because of their inherent shielding features and minimal crosstalk with other nearby transmission lines or components. Electromagnetic waves are tightly confined between signal paths and the adjacent ground planes, which prevents antenna radiation from being interrupted and degraded. The GCPW approach also enables designers to control and achieve a wide variety of impedances simply by adjusting the spacing between the grounds and the signal line without changing the thickness of the dielectric. The partial ground plane in M2 is incorporated for the GCPW signal distribution. In mm-wave frequencies (20 GHz and above), dielectric loss in multi-layered signal routing dominates the package loss budget, requiring low-loss-tangent (tan δ) dielectric materials to maintain the signal integrity and mitigate signal losses in the package.

The partial ground plane placed in M2 is interconnected to the ground plane in M3, which serves as a ground plane for the Yagi-Uda antenna and GCPW signal traces in the M4 layer. The GCPW formed in M4 is interconnects to TPVs as a feed line of the Yagi-Uda antenna. The signal TPVs are surrounded by two grounded TPVs, where the impedance of TPVs is controlled by changing the pitch between the signal and ground TPVs. The impedance control in TPVs is critical to achieve impedance matching and high bandwidths of package-integrated antennas. Specifically, the GCPW alone (Figure 4.4a) is designed to be slightly capacitive and less resistive than the target impedance since TPVs usually add more resistance and inductive reactance (Figure 4.4b). The characteristic impedance of the GCPW is therefore designed to be $(46 - j0.44)\,\Omega$. The designed GCPW consists of a signal width of 27 μm with a space of 44 μm with a 15-μm build-up dielectric (ABF GL102: Dk = 3.3, Df = 0.0044 at 5.8 GHz).

The landing pads on the package side, interconnecting dies and discrete passive components (e.g., bypass capacitors), are designed to have a diameter of 120 μm, where as the solder ball size is approximately 80 μm on a pitch of 200 μm. The dies and passives are flip-chipped underneath the M4 layer to hinder those assembled components from inter-

fering with the Yagi-Uda antenna and to effectively miniaturize the package, as shown in Figure 4.3. Direct current (DC) voltage with a bias of 5V is supplied from the M4 layer while bypass capacitors of 0.1 μF and 100 pF are mounted no farther than 0.7 mm from the LNA to short AC signals to ground producing clean and pure DC signal.

4.1.2 Process Development

This section discusses the development of the process and chip assembly methodology to form circuitry to provide high-density low-loss interconnects and high precision of RDLs on core substrates.

Thin alkali-free boro-aluminosilicate glass core substrates with vias pre-drilled by AGC Inc. (formerly Asahi Glass Co., Ltd.) are employed for the test vehicles. The through-glass vias (TGVs) were designed to have a diameter of 80 μm. Six-inch square panels with 100-μm thickness are used for the process demonstration. This technology is compatible with large-area panel packaging, which is widely being commercialized recently [111, 112]. It potentially allows to obtain 4.54 times more coupons on a panel of 500 mm $\times$ 500 mm size, which also lowers the cost compared to a traditional 12-inch round wafers used for fan-out wafer-level packaging. Appropriate handling procedures are critical for glass substrate fabrication processes to address the brittleness and fragility of ultra-thin glass. The lamination of thin dielectric films is the key to compensate for the brittleness of thin glass substrates. The dielectric properties are listed in Table 4.2. Notably, the adhesion of dielectric materials for build-up layers to copper metal patterns and glass substrates is improved, compared to the test vehicles in [23, 8]. The fabrication process of the high-density RDL interconnects is summarized in Figure 4.1 and discussed in [23, 113] with more details.

Upon the completion of multi-layer fabrication on glass cores laminated with thin-film dielectrics, solder-resist films provided by Taiyo Ink. are laminated on both sides of the package substrate to prevent the outermost surface from being oxidized or damaged. This

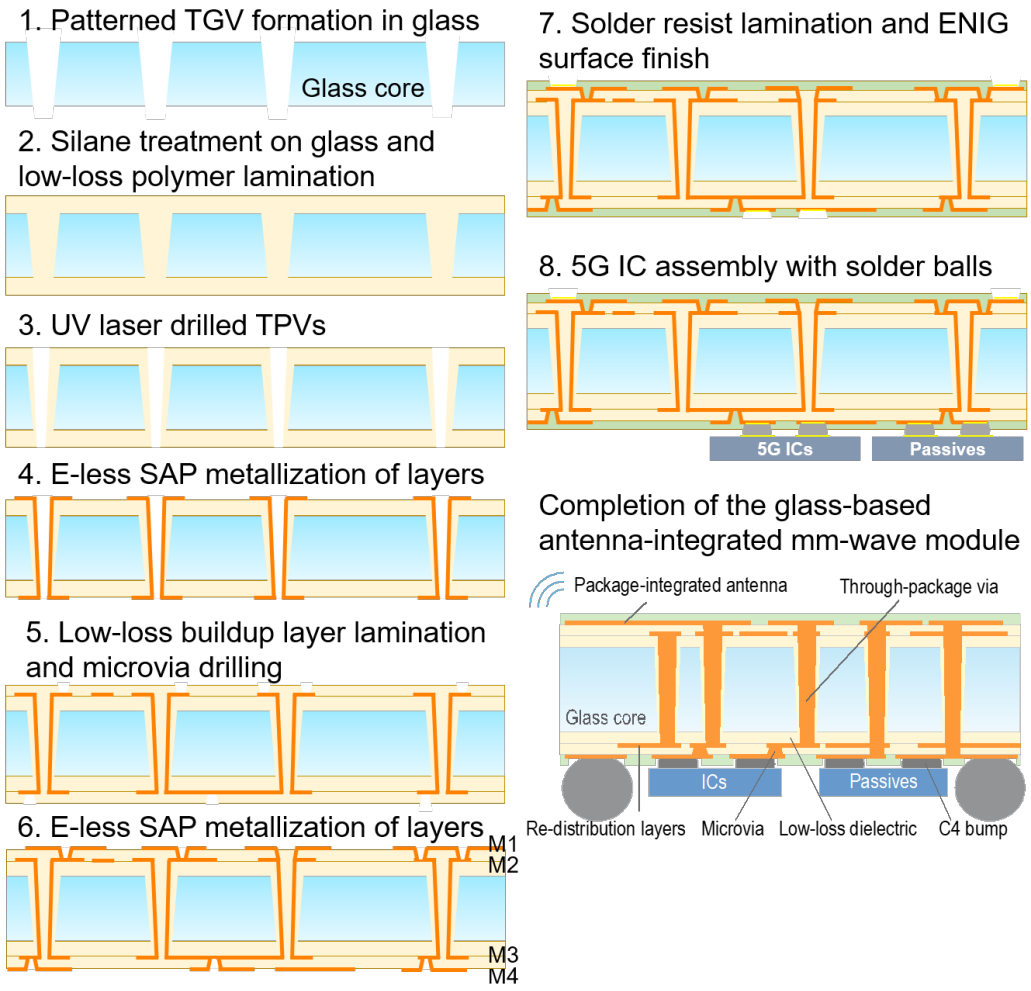

Figure 4.1: Fabrication process of highly-integrated mm-wave packages with the via-in-via process, RDL formation, and the assembly of ICs and passive components.

process is also depicted in Figure 4.1. We designed solder-mask-defined (SMD) chip-to-package interconnects to reduce the size of the copper pads that the component is soldered to. To prevent oxidation of copper traces and pads and suppress intermetallics formation, a thin layer of electroless-nickel immersion gold (ENIG) is deposited, followed by the placement solder balls with a diameter of 80 μm approximately on 80-μm pads with 200 μm pitch. The GaAs-based dies are assembled with a flip-chip tool, while several passive components such as bypass capacitors are surface-mounted with solder paste. The solder balls and solder paste are reflowed altogether at the end of the fabrication. The cross-section images with TPVs and dies assembled as such, are shown in Figure 4.2, while the top-view

inspection is performed through an X-ray microscope and the image is depicted in Figure 4.3.

Table 4.2: Material properties utilized in the 3D glass-based antenna module.

Materials	Glass core	Build-up dielectric
Dk	5.4	3.3
Df	0.006 @ 28 GHz	0.0044 @ 10 GHz
CTE (ppm/K)	3.8	49
Thickness (μm)	100	15

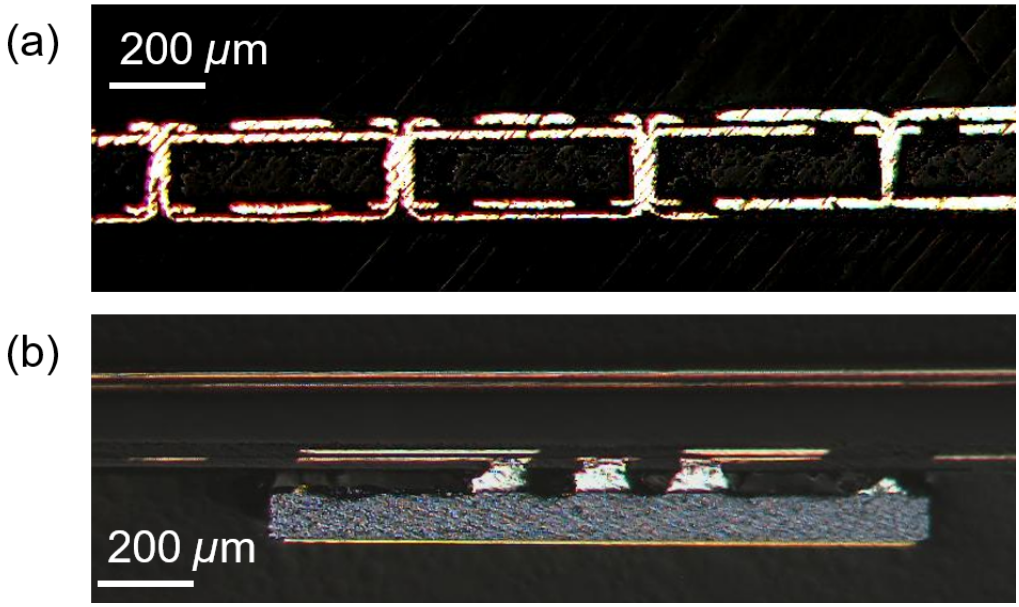

Figure 4.2: Microscope cross-section images of fabricated panel with the four re-distribution layers, (a) through-package vias, microvias, (b) an assembled LNA using 80-μm solder balls.

4.1.3 Characterization of Key Building Blocks

To characterize the fabricated four-metal-layer glass substrate test vehicle, high-frequency measurements of transmission lines and TPVs as interconnects, package-integrated Yagi-Uda antenna, and a flip-chip-assembled LNA are performed through a vector-network analyzer (VNA) that is calibrated up to 40 GHz.

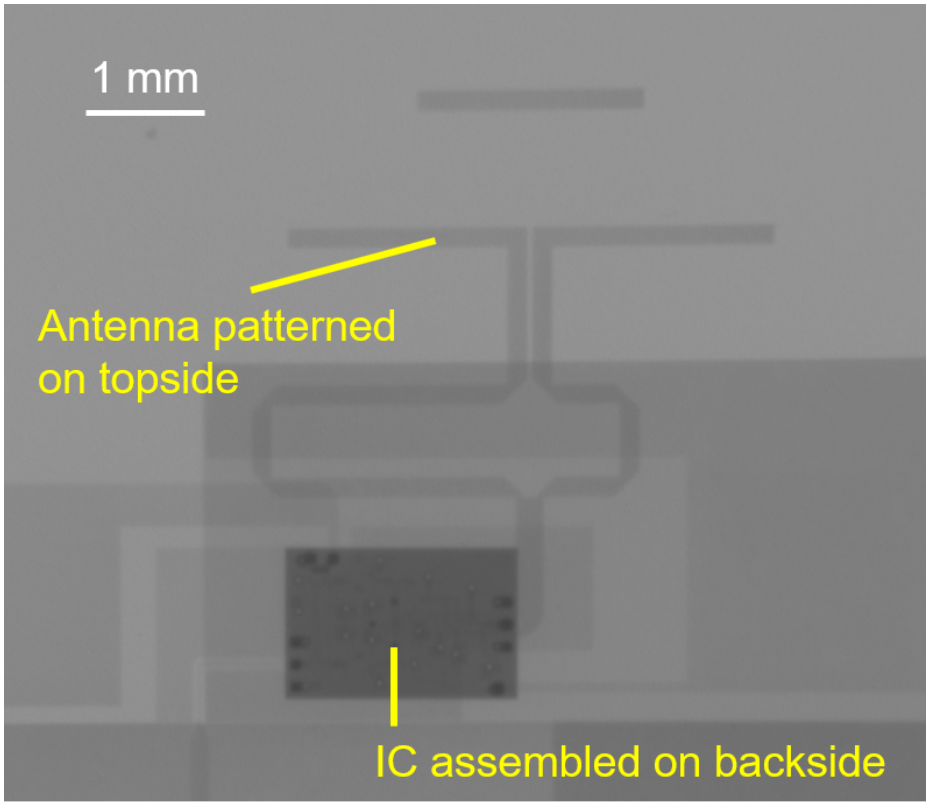

Figure 4.3: X-ray inspection of the test vehicle that integrates a Yagi-Uda antenna, impedance-matched interconnects, through-package vias, and an assembled LNA.

Characterization of Low-Loss Interconnects

While the copper thickness is 8 μm in all the layers of this package, the width and space of the designed GCPW were 27 μm and 44 μm, respectively. However, the photomask for lithography was designed differently, considering over-etching of metal patterns. As the typical semi-additive patterning (SAP) processes over-etch approximately 0.5 μm – 1 μm, the width and space became 29 μm and 42 μm on the photomask. As designed from the electrical and process standpoints, the fabricated GCPW showed the precise line width and space, which are 27.3 μm and 43.3 μm, respectively, as shown in Figure 4.4(a). Based on the fabricated interconnect structures (Figure 4.5), S-parameters were measured to quantify the signal losses induced by the interconnects between the antenna and IC. The interconnects include 2-mm GCPW and 2 TPVs (Figure4.4). The S-parameters for the

structures with and without TPVs are plotted in Figure 4.7. As discussed in Section 4.1.1, GCPWs are formed in M1 and M4 interconnected with TPVs.

While the article [8] shows the insertion loss of transmission lines on a 100-μm glass substrate in the narrow bands (26 – 30 GHz) with poor impedance matching with rippled frequency responses, the characterization results in this research presents impedance-matched GCPWs and TPVs to the 50-Ω system, leading to low voltage standing-wave ratio (VSWR) in the target frequency range (24.25 GHz – 29.5 GHz). In addition to the pad-to-via impedance continuity, the impedance of TPVs is adjusted by manipulating their diameter (50 μm) and the pitch (200 μm). In addition to the low insertion loss, the results (Figure 4.7) indicate the return losses of higher than 20 dB in the whole frequency band of interest (22 – 30 GHz). The Smith chart, Figure 4.6, also shows the well-matched input impedance for both the GCPW line and the chain of GCPW and TPVs. While the real parts of their input impedance are close to 50 Ω, the reactance of the structure with TPVs is 7.04-Ω higher in measurements, which is attributed to the inductive parasitics from TPVs [114]. However, the design with consideration of the inductive effect assisted the impedance of the chain with TPVs to match 50 Ω, resulting in the low return loss higher than 20 dB in the entire frequency range of interest.

The measured insertion loss of GCPW with solder resist without TPVs was 0.216 dB/mm at 28 GHz. The simulated insertion loss of GCPW alone is 0.119 dB/mm without the solder resist. The addition of solder resist leads to the simulated insertion loss of 0.178 dB/mm at 28 GHz. This 50% increase is mainly attributed to the loss tangent of solder resist (Df = 0.02 at 1 GHz). Thus, it is critical to design circuitry in outer layers considering the properties of a solder mask. The evident signal loss due to solder resist leads to a demand for low-loss solder resist for mm-wave applications.

Based on the measured GCPW insertion loss, the insertion loss caused by TPVs was measured by subtracting the insertion loss of the chain (Figure 4.4b) from GCPW (Figure 4.4a), in which the length of the GCPW is kept identical. The measured TPV loss was

0.021 dB/TPV. The controlled diameter of landing pads and anti-pads (Figure 4.5b) also affect the signal transition from the electromagnetic-wave standpoint. Compared to traditional through-hole vias in multi-layered organic substrates, where comparatively large vias ($> 500\,\mu$m) are drilled mechanically, through-glass vias with the via-in-via process are beneficial in achieving smaller dimensions (i.e., diameters and pitches) with better control for high-density interconnects to manage signal integrity.

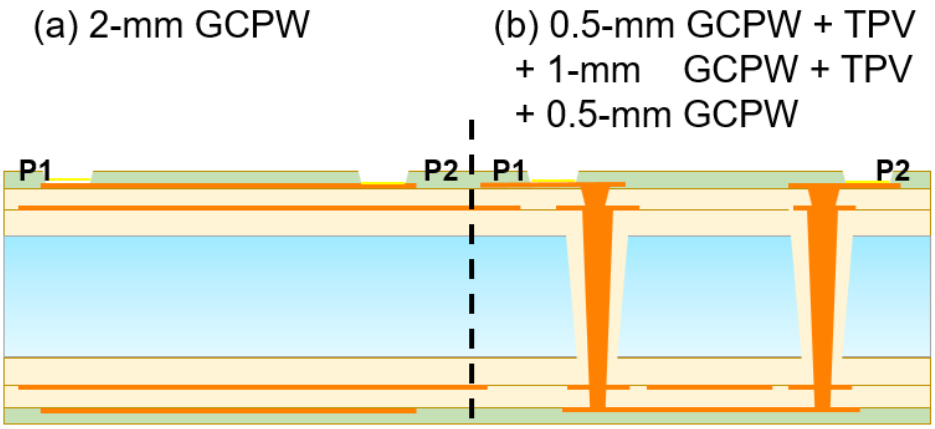

Figure 4.4: Design and stack-up of several interconnects used in this test vehicle (a) Transmission line (b) Transmission lines with TPVs.

The via-in-via process in glass substrates connects multiple layers without the need for re-routing signal traces in-plane and vertically-connecting RDLs with blind vias. The TPV in Figure 4.5c interconnects the top metal layer (M1) to feed antennas and the second bottom layer (M3) directly. This advantage offers space reduction for signal routing, seamless impedance continuity, and design flexibility to RF designers. Glass substrate technology offers highly-accurate layer-to-layer alignment, which enables the pad size closer to the diameter of vias. The small via pads and spacing lead to low parasitic capacitance between via pads in multiple layers and low impedance discontinuity. The fabricated test vehicle, as depicted in Figure 4.5b, shows the margin of 10 μm on either side of TPVs.

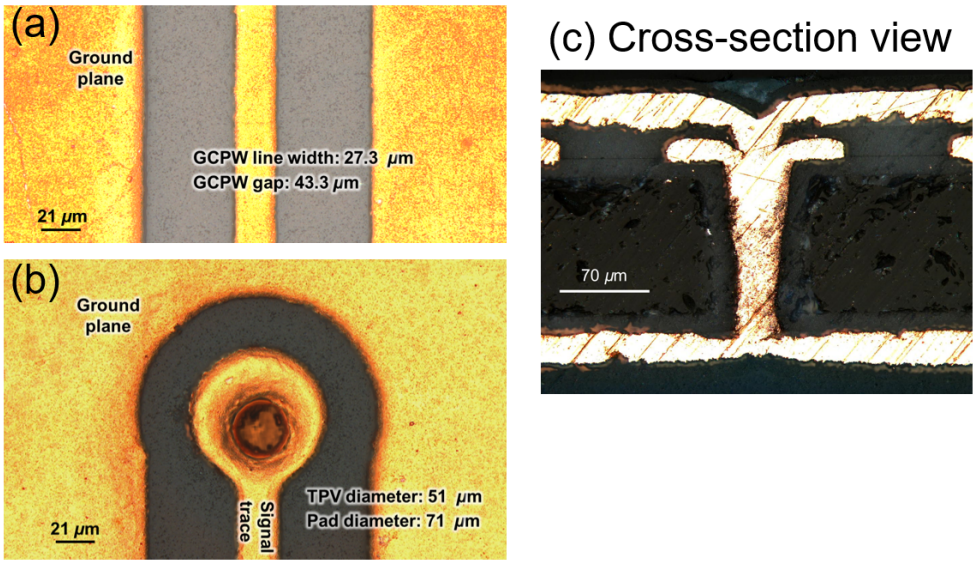

Figure 4.5: Package-level interconnects (a) Top view of ground-backed co-planar waveguide (GCPW) (b) transition from GCPW to TPV (c) Cross-section view of TPV connecting M1, M2, and M3 altogether.

Characterization of Yagi-Uda Antenna on Glass

The designed Yagi-Uda antenna is shown in Figure 4.8a with the detailed parameters of the antenna, which are listed in Table 4.3 with their values. While the fabricated antenna is depicted in Figures 4.8b and 4.8c, the 3D view for simulations is illustrated in Figure 4.9a along with the radiation pattern in Figure 4.9b. To characterize the fabricated Yagi-Uda antenna that is patterned on thin-film dielectric (M1) laminated onto the glass core, the panels were first singulated utilizing an automatic dicing machine (Disco Corporation), and a 2.92-mm end-launch connector was mounted onto the feed line connected to a Yagi-Uda antenna patterned on the top layer of the package, as shown in Figure 4.8. Figure 4.10 depicts the in-plane (E) and out-of-plane (H) radiation patterns of the single-polarized Yagi-Uda antenna, with a comparison between the simulations and measurements. The main lobe is more directive in the E plane because of the linear-polarization feature of the antenna, while the radiation patterns in the H plane are wide-angled. The radiation patterns in the E and H planes show good consistency at 25 GHz and 28 GHz. It is critical for

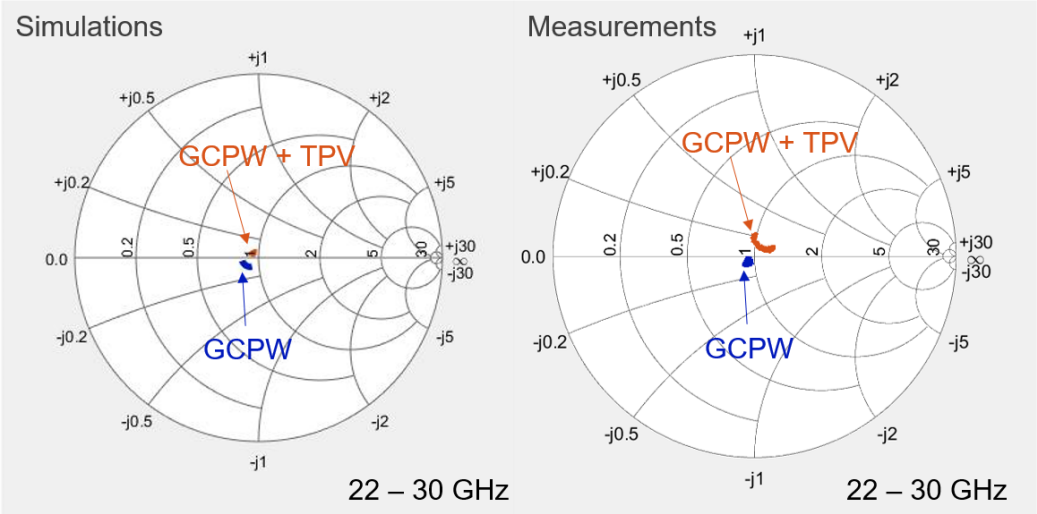

Figure 4.6: Smith chart showing return losses from GCPW and the chain of GCPW with two TPVs in the frequency range from 22 – 30 GHz.

antennas to show similar radiation patterns throughout the frequency band of interest for versatile usage of those antennas in electronic devices.

The simulated and measured return losses of patterned Yagi-Uda antennas are plotted in Figure 4.11. The Yagi-Uda antenna is designed to have double resonances to increase the bandwidth. One null at 22.3 GHz comes from the dipole, while the other null at 27.1 GHz results from the quarter-wave transformer. This double resonance resulted in the 10-dB return losses in the frequency range, 21.9 – 29.8 GHz, with a center frequency of 25.85 GHz. This indicates that the Yagi-Uda antennas fabricated on the 100-μm glass substrate cover the entire frequency band of interest used for 28-GHz-based 5G communications (24.25 – 29.5 GHz). The fractional bandwidth is 28.2% around 28 GHz, supporting the key frequency spectra (n257, n258, n261) in the Frequency Range 2. Notably, the three Yagi-Uda antennas randomly selected from the fabricated glass panel show high repeatability of return loss. This high repeatability results from the high precision of fabrication enabled by the dimensional stability, thickness control, and surface flatness of glass substrates. The observed deviation in the smallest feature, 25 μm, was less than 2 μm with a high accuracy of the layer-to-layer alignment.

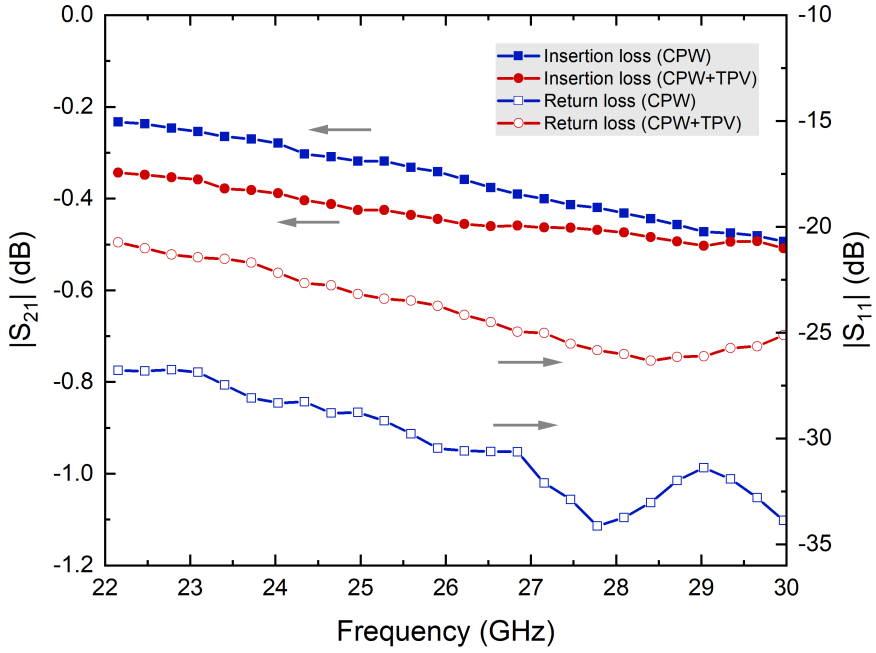

Figure 4.7: Measured S-parameters of the glass-package interconnects with and without TPVs.

The realized gain is measured using a standardized octave horn antenna which shows a realized gain of 20 dBi and covers a frequency range of 18 – 40 GHz. The measured realized gain of the fabricated Yagi-Uda antenna is plotted in Figure 4.12. The result showed a good model-to-hardware correlation and a realized gain higher than 3.44 dBi in the targeted frequency bands.

Table 4.3: Parameters used for the antenna design

Parameters	Values	Parameters	Values
w_{ant}	180 μm	w_{bal}	180 μm
d_{dir}	1.18 mm	l_{bal}	0.82 mm
d_{gnd}	1.09 mm	w_{ant}	220 μm
s_{cps}	50 μm	l_{ant}	2.2 mm
w_{cps}	180 μm	w_{ant}	180 μm

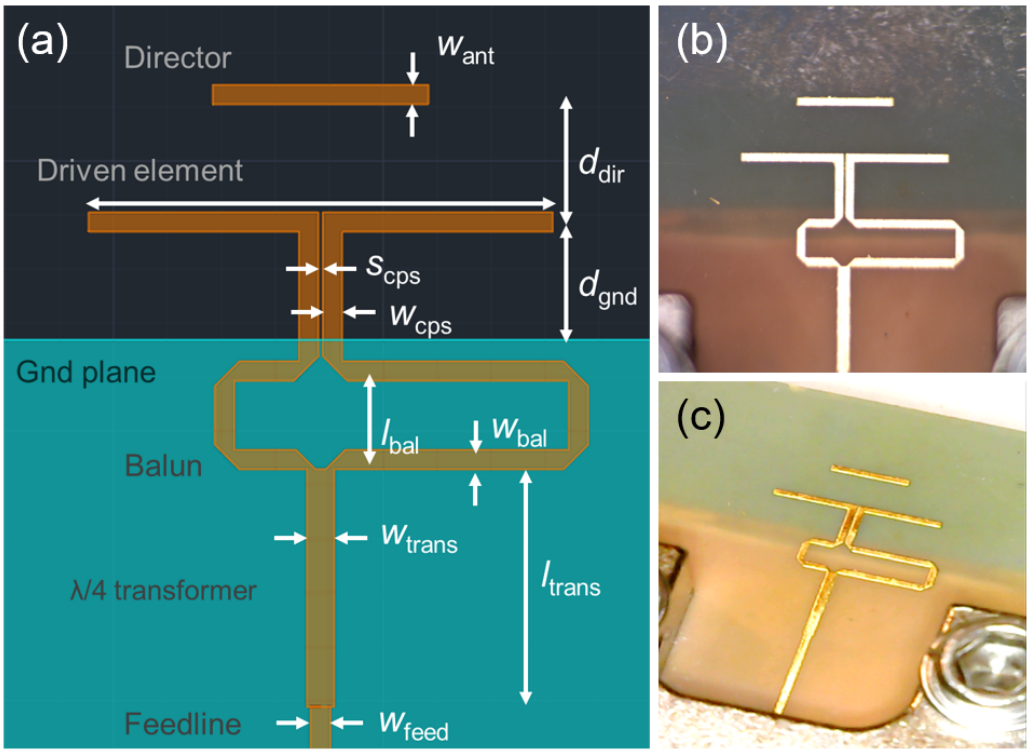

Figure 4.8: Fabricated package-integrated Yagi-Uda antenna (a) Overview with key parameters (b) Top overview of the antenna (b) Diced Yagi-Uda antenna element assembled with a 2.92-mm end launch connector.

Characterization of Flip-Chip-Assembled LNA

In RF receiving architectures, signals from antenna arrays are delivered to LNAs to amplify the very low-power signals that are received from the antenna. Package-level interconnections assist ICs and packages to communicate with each other and to external interfaces. In order to address the trend toward high-frequency networks, higher number of I/Os are required to enable complex beamforming, higher data rate, and faster signal processing. Advances in IC design with system-on-chip (SoC) technology along with ultra-short die-to-package interconnections with low signal losses are required to realize the high-frequency modules. Solder-ball assembly technology is often utilized as the mainstream option for RF packages due to its cost effectiveness and the self-alignment feature during reflow assembly. Although the copper-post interconnection solutions, which are mainly employed for high-performance computing, provide lower signal losses due to the higher conductivity of

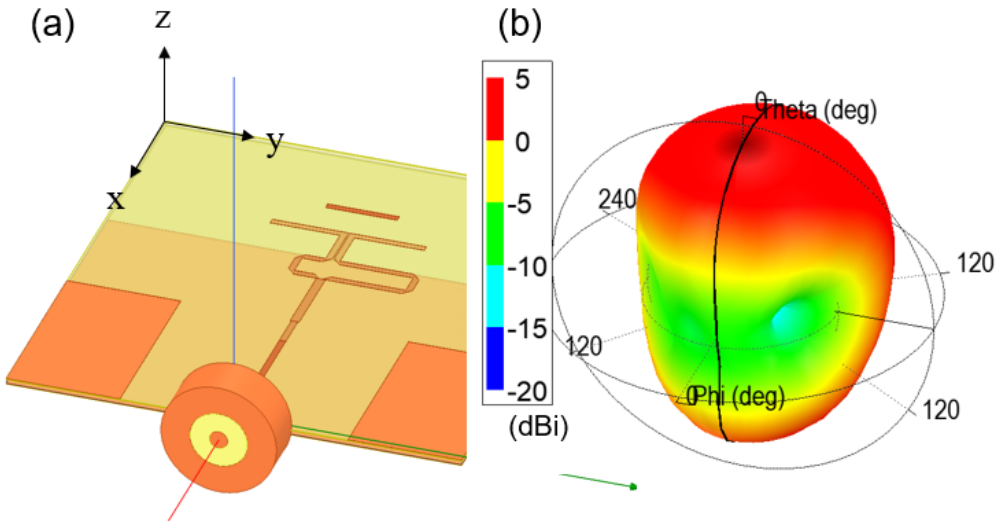

Figure 4.9: Designed wide-band package-integrated Yagi-Uda antenna (a) 3D overview of the antenna (b) simulated radiation pattern.

copper than that of solder, the approach is not considered cost-ineffective and impractical for RF packages. In this test vehicle, flip-chip interconnection is demonstrated with solder balls with a diameter of 80 μm whereas the pitch of solder-mask-defined (SMD) pads is 200 μm, which gives enough space to prevent solder balls from shorting. In order to show short and fine-pitch interconnections using solder balls with low insertion loss, the assembly of LNA and bypass capacitors is performed with solder reflow assembly, also known as controlled collapse chip connections (C4). The assembled LNA is a product of Analog Devices [118], which covers the frequency range of 24 – 40 GHz.

Optical micrographs of the flip-chip assembled LNAs are depicted in Figure 4.13. State-of-the-art RF packages employ a pitch of 200 – 300 μm with a solder-ball diameter of approximately 80-100 μm [12, 29]. The measured forward voltage gain, S_{21} is plotted in Figure 4.14 with intended voltage (5 V) and current (0.065 – 0.07 A) supplied to the packed LNA, as shown in the inset of Figure 4.14. The measured result showed positive gains in the entire frequency band of interest. Especially at around 28 GHz, the gain is observed to be higher than 10 dB and is 20 dB at maximum. The LNA, which was flip-chip mounted onto the glass-based package, is originally designed by the manufacturer

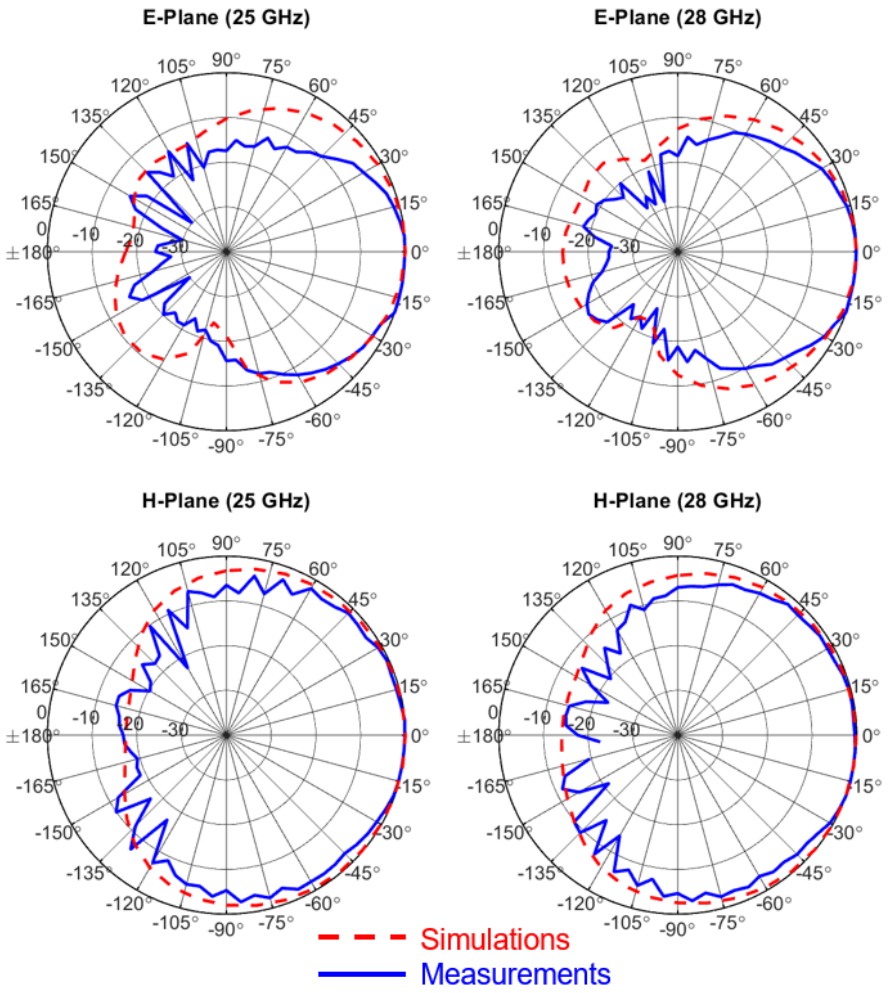

Figure 4.10: Simulated (red) and measured (blue) in-plane (E) and (H) radiation patterns with normalized gains. The director of the Yagi-Uda antenna is placed in the direction of $\theta = 90°$ and $\phi = 0°$.

to be wire bonded, where the LNA is faced up. This selection of LNAs designed for flip-chip modules could provide flat gain across the whole band of interest. It is, therefore, re-iterated that the co-design of integrated ICs, antennas, and their packaging is critical to obtain optimal performance in front-end modules.

4.1.4 Comparison

The comparisons between the proposed work and previously-reported results are summarized in Table 4.4. The parameters associated with the antenna performance are based on

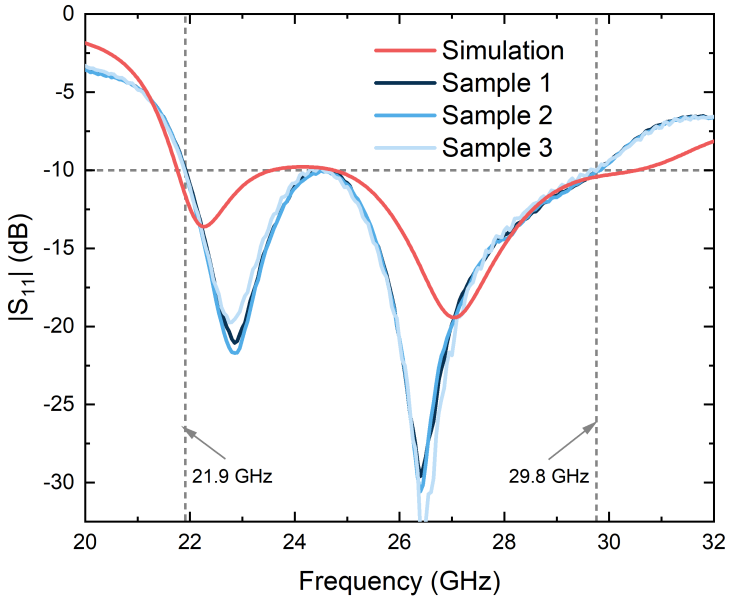

Figure 4.11: Measured return loss of three antennas fabricated in the four-metal layered test vehicle to validate the consistency of frequency responses of the antennas across the glass panel.

a single antenna element. Key substrate technologies (PCB, LTCC, multi-layered organic, and glass) with integrated antennas operating at 5G frequency bands are benchmarked for comparison. As shown in Table 4.4, the proposed work covers the important frequency bands around 28 GHz (n257, n258, n261) with the thinnest substrate (100 μm). The relative thickness in the proposed work, shown in the table, includes the thickness of assembled die (100 μm), the bump height (50 μm), and the height of the solder resist and multi-layers formed on the core substrate, which results in 300 μm in total ($0.028\lambda_0$ at 28 GHz). The proposed work also demonstrated horizontal and vertical interconnects with solder resist patterned for IC assembly.

4.1.5 Summary

This section presents heterogeneous integration of antenna-in-package, seamless or low-loss antenna-to-receiver signal transitions, and flip-chip assembly on ultra-thin glass

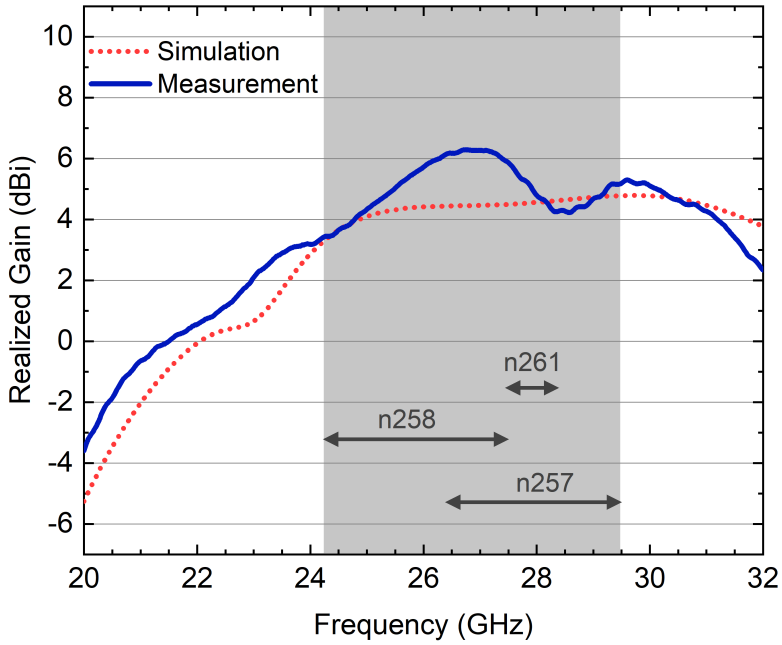

Figure 4.12: Realized gain of the fabricated antenna in the direction of $\theta = 90°$ and $\phi = 180°$.

substrate panels, in the 28 GHz band for high-speed 5G communication standards. The key benefits of glass core such as dimensional stability, thickness control, unique laminated glass stack-up, and via-in-via processes result in process stability and design flexibility for system design. Module-level characterization results highlight the low interconnect signal losses with a through-package-via loss of 0.021 dB/TPV at 28 GHz. The Yagi-Uda antenna fabricated on glass substrates showed a center frequency of 25.85 GHz with a fractional bandwidth of 28.2%, which covers the 28GHz 5G frequency bands of interest. The antenna also featured a wide-angle main lobe at the target frequency range, implying good coverage of signal transmission and reception. Overall, this article reports package-integrated antenna, feedlines, low-loss interconnects, and assembly of active ICs and discrete passive components implemented with 100-μm glass-substrate technology.

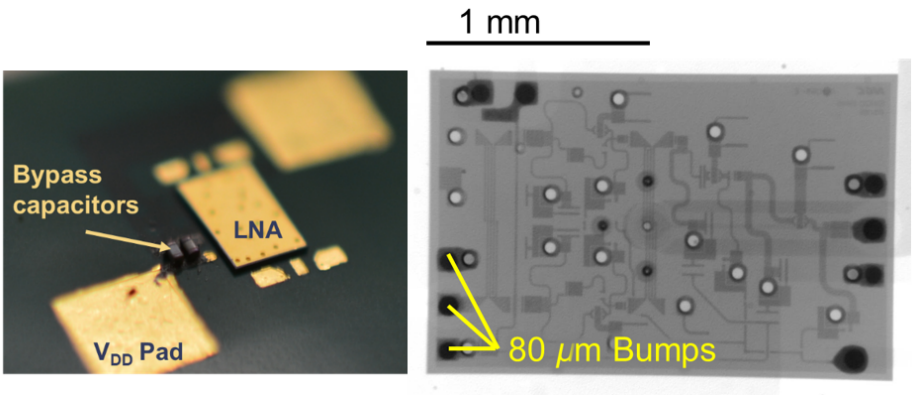

Figure 4.13: 3D view of the backside of the package (left) and X-ray inspection of solder balls mounted on SMD pads (right).

4.2 Glass-Based IC-Embedded Antenna-Integrated mm-wave Packages

4.2.1 Process Development of mm-wave Glass-Panel Embedding Stack-up

The overall fabrication flow of die-embedding into glass substrates is illustrated in Figure 4.15, along with the RDL formation to interconnect integrated components and feed antenna patterned on the front side of the package. Detailed process steps are discussed in this section.

Through cavity formation in glass substrates

Although glass substrate technology is becoming essential in a wide variety of applications such as RF, photonics, and micro-electromechanical system (MEMS), micromachining glass still remains technically-challenging due to poor machinability. In addition, it requires major investments to manufacture. There are four approaches to glass micromachining: mechanical, thermal, chemical, and hybrid machining, among which thermal machining through laser ablation is the most suitable method for fast in-house prototyping. The laser used for through-cavity formation in glass substrates in the research is OPTEC WS-Flex USP system with a pulse width down to 221 femtoseconds. The equipment utilizes laser of a wavelength of 1030 nm, at which glass is transparent. However, the

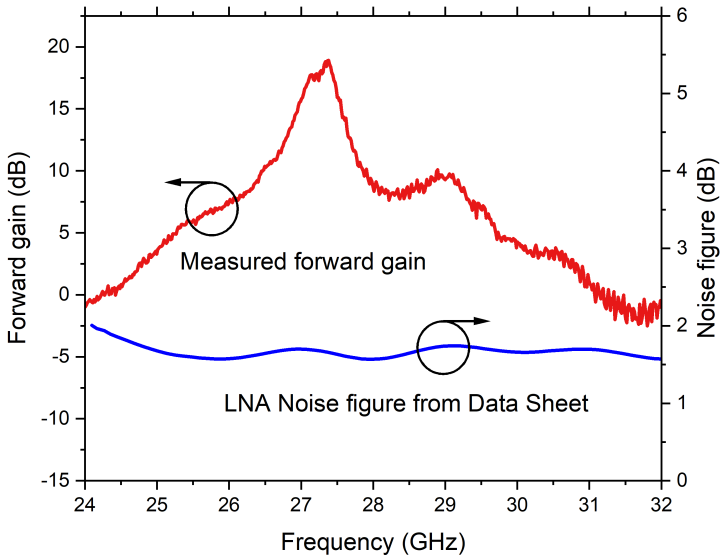

Figure 4.14: Forward insertion loss, S_{21}, of the flip-chip-assembled LNA with bypass capacitors surface-mounted nearby. The inset figure shows the voltage and current supplied to the packed LNA.

ultra-short laser pulses in the system provide extremely-high peak intensity which provides absorption through nonlinear processes, leading to effective ablation in glass.

By adjusting the laser power, frequency, pulse pick divider, repetition, and galvo scanner speed, the laser system is optimized for fast and high-quality glass cutting processes. The drilling process is set up as the following:

1. Focus the laser beam on the surface of the glass substrate.
2. Drill a trench along the rectangular perimeter of the designed cavity.
3. Drill additional rectangles inward to form a larger opening in the same layer.
4. Move the laser downward and refocus the laser at the bottom of the opening.
5. Repeat step 2, 3, and 4, until the laser focal plane reaches the bottom of the glass.

Once the process is completed, the isolated glass piece in the drilling pattern will fall off automatically, which results in a through cavity in glass (Figure 4.15b). As the glass cavity

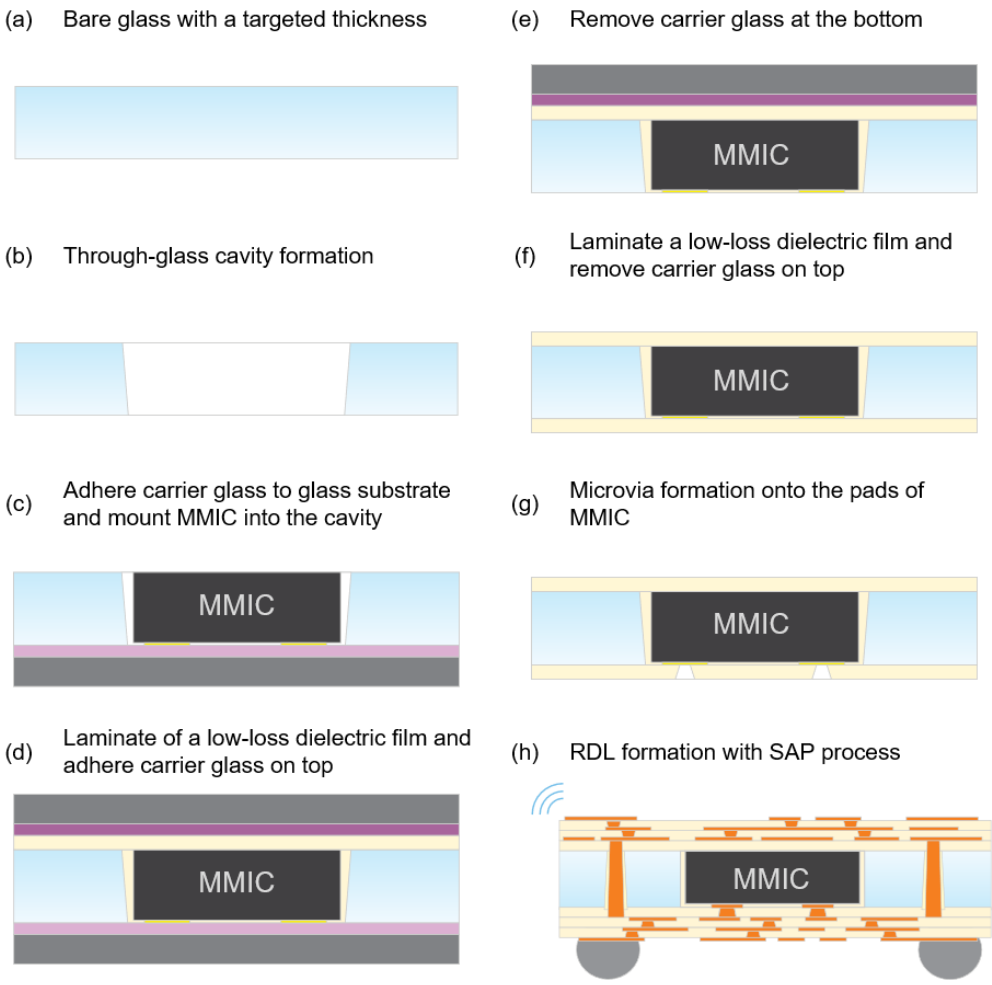

Figure 4.15: Process flow of Glass Panel Embedding (GPE) for 5G mm-wave antenna-integrated packages.

exhibits tapered side walls of 45 – 60°, the top opening was designed to be 400 μm larger than the MMIC size (2.1 mm $\times$ 1.37 mm). The bottom opening of the glass substrate has a 100-μm gap on each side of the die to be embedded. The thickness of the glass substrate and the MMIC was designed to be identical (approximately 120 μm). The top view of the drilled through-glass cavity is shown in Figure 4.16a. The cavity profile on each side is measured with a profilometer and plotted in Figure 4.18.

Die placement in cavities

Upon completion of the glass-cavity drilling and adhesion of the 1.1-mm thick glass carrier to the bottom (Figure 4.15c) using a temporary release film provided by Nitto Denko, an un-bumped MMIC, which is a GaAs-based LNA, is assembled using the Thermocompression Bonding (TCB) process utilizing a Fintech Semi-Automatic Bonder. A low-loss 28-μm dry film, which is provided by Taiyo Ink., is laminated to the top of the package and is cured at 110°C to encapsulate the mounted die and to fill the gap. The un-bumped die with gold surface finish over the pad terminator is faced down (Figure 4.15c) so that the dielectric thin film at the bottom does not exhibit dimples after the lamination of the thin film. The dimples around the die pose risk of the failure of precise via formation and metal patterning. The bottom view after the double-side dielectric lamination (Figure 4.15g) is shown in Figure 4.16b.

The cross-section image of such an embedded dieis shown in Figure 4.17 after the completion of the embedding (Figure 4.15g). The result indicates that the MMIC is successfully embedded into the drilled glass cavity and the low-loss dielectric thin films holds the IC properly. The dark-colored cracks observed in the 120-μm glass were generated during the cross-sectioning of the fabricated test vehicle. The measured surface profile (Figure 4.18: red curves) exhibits the smooth-surface on the pad side of the die, which facilitates the SAP processes for RDL formation (Figure 4.15h) to fan-out signal traces, bandpass filters, and antennas.

4.2.2 Electrical Elements Integrated in the Package

As wavelengths becoming shorter with the high-frequency spectra, heterogeneous integration is the key in mm-wave antenna-integrated packages to enable high-gain high-bandwidth antennas, minimize signal losses while maintaining the signal integrity, and address the form-factor challenge. This section begins with the study of the signal losses and impedance matching in IC-to-trace interconnections of the chip-embedding structure,

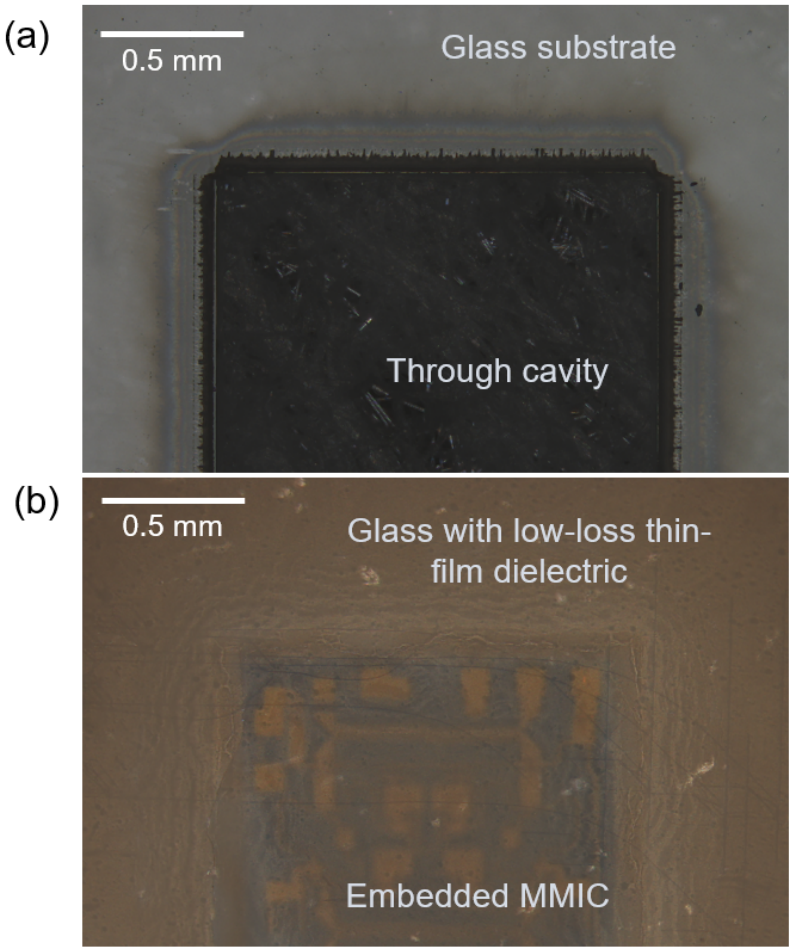

Figure 4.16: Top view of (a) the glass through-cavity drilled with the femtosecond laser and (b) the die-embedded glass package.

comparing to the flip-chip technology (Section 4.2.2). A bandpass filter is also integrated into the test vehicle, and its technical challenge and performance are introduced in Section 4.2.2. Following the bandpass filter discussion, the design and electrical performance of dual-polarized package-integrated antenna is discussed in Section 4.2.2.

Interconnects in the package

Short interconnects and impedance matching between the IC and components such as antenna or a filter are critical to enhance the performance of the components [119]. To quantify the signal losses caused by two different assembly methods, the chip-embedded

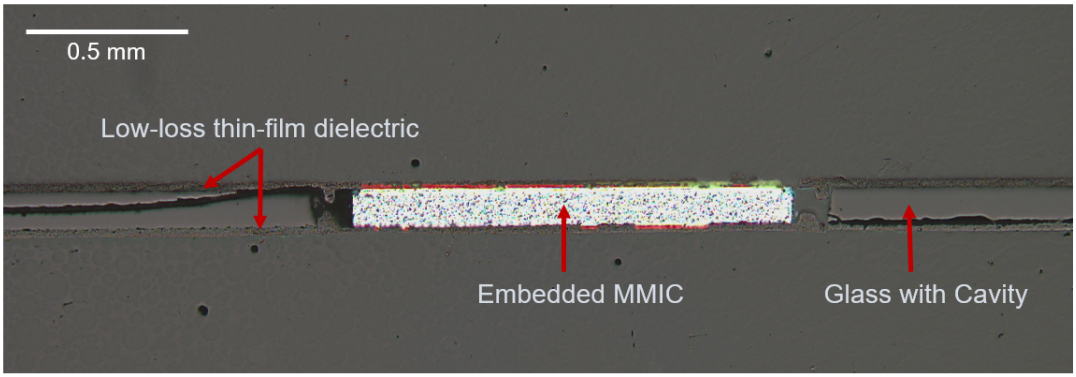

Figure 4.17: Cross-section image of the MMIC-embedded glass package.

structure in glass and the flip-chip assembled die based on C4 bumps were modeled as shown in Figure 4.19.

Figure 4.20 shows the return loss and the insertion loss of the two different assembly interconnections with co-planar waveguides (CPW), simulated in a 3D full-wave solver. The comparison between the C4-bump interconnection (flip-chip) and the microvia interconnection (IC-embedding) indicates that the signal loss induced by the microvia interconnects is at least 3X lower than the one caused by the flip-chip interconnection. This reduction results from the shorter interconnect of the microvia, which is equal to the thickness (15 μm) of the dielectric that encapsulates the die, while the solder-ball height is approximately 80 μm for 100-μm pads on the die. Another factor is the low dielectric loss (Df = 0.0025) around the microvia interconnections, while the solder balls are surrounded by solder resist or underfill that have relatively-high dielectric loss tangent (Df = 0.02). The return-loss comparison plotted in Figure 4.20 implies that the other key factor is the ease of impedance matching with the microvia interconnections. The deviation of the dielectric constant of solder resist leads to undesired impedance, resulting in higher return loss or standing wave ratio. The microvia interconnections, in contrast, facilitate to control the diameter and enable high-density interconnections because of the capability to form sub-5 μm microvias [106].

An MMIC, which is a GaAs-based LNA covering a frequency range of 24 – 40 GHz

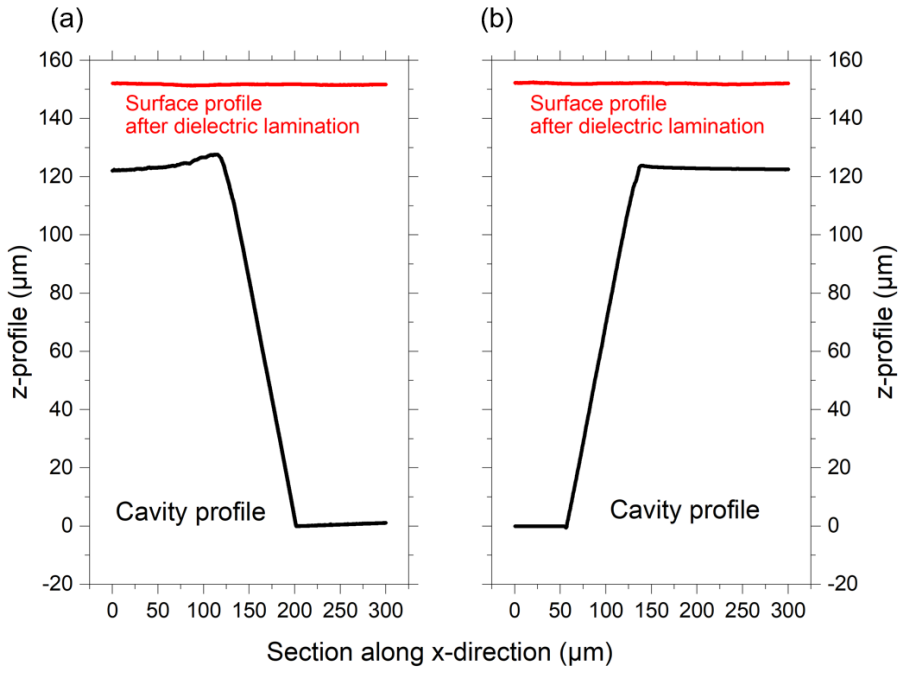

Figure 4.18: (a) Left corner and (b) right corner of cavity profiles after femtosecond-laser drilling and the surface profile after the dielectric lamination on the backside of the package.

in this research, is computed in a circuit simulator to compare the S-parameters with and without the microvia interconnects. The cross-section image is shown in Figure 4.21. The simulated S-parameters are plotted in Figure 4.22, indicating that the LNA frequency responses are not degraded by the microvia chip-to-package interconnects. This is attributed to the low insertion loss and matched impedance of the microvias (Figure 4.20) to the input and output of the LNA (50 Ω).

Bandpass filter implementation

With the increasing demand of frequency spectra and increasing carrier-aggregation bands, more band filters are required. This trend puts pressure on filter design and ramps up its design and fabrication complexity as multiple-input multiple-out (MIMO) systems expand with increasing consumer demands. Conventionally, mm-wave components are implemented on chip because of the tight process tolerance. However, on-package band filters are also gaining attention because of the potential to offer high-Q and the cost effectiveness

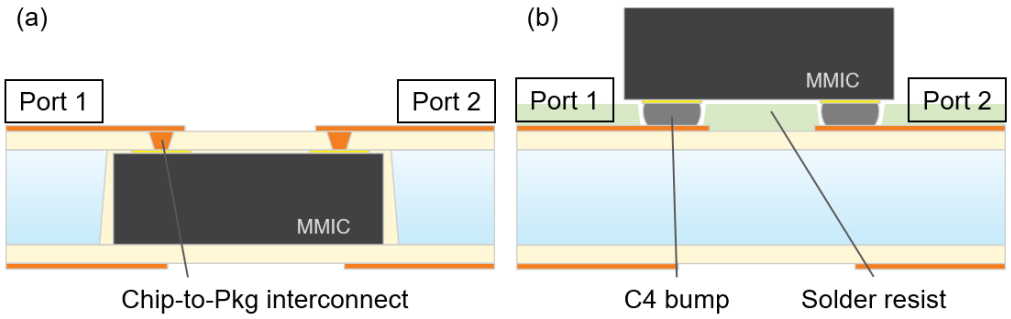

Figure 4.19: Modeled assembly methods: (a) Chip-first glass-panel embedding with microvias and (b) Chip-last solder-ball-based flip-chip with solder resist.

[120].

Bandpass filters (BPF) in the designed test vehicle are incorporated between the antenna and an LNA, as shown in Figure 4.23. The interdigital-structure BPF is employed for the n257 band (26.5–29.5 GHz), which is integrated at the bottom of the package. The placement of the filters below the ground plane for the antenna, as shown in Figure 4.27, mitigates the degradation of radiation patterns of the antenna located on the front side of the package. Interdigital filters use quarter-wavelength ($\lambda/4$) short resonators, which leads to small footprint in packages. The resonator for interdigital filters has fixed width and the spacing between resonators, as depicted in Figure 4.24a, is adjusted to obtain the required frequency response. The passband is defined by 3 dB, as plotted in Figure 4.24b, and the frequency band for the filter was selected based on the frequency range that the package-integrated patch antenna covers, which is the 5G New-Radio (NR) n257 band defined by 3GPP. More details on the RDL-level filters are discussed in [113, 120].

Package-integrated antenna

The use of dual-polarized antenna, which receives or transmits electromagnetic waves with two orthogonal polarizations, is significant to increase the traffic handling capacity of systems in a given physical area [121, 122]. A dual-polarized patch antenna is designed and integrated into the glass-based chip-embedded package, as illustrated in Figure 4.27. The

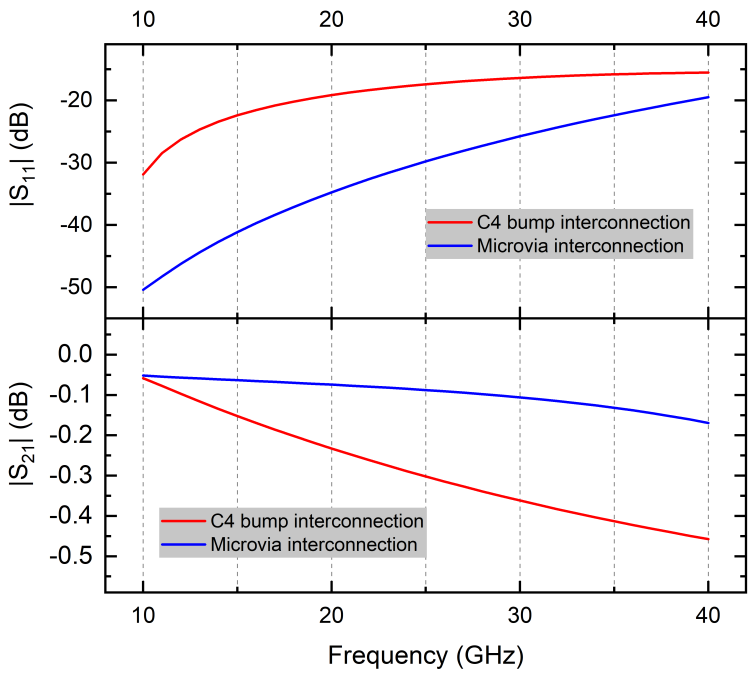

Figure 4.20: Return loss and insertion loss based on C4-bump interconnection (flip-chip) and microvia interconnection (IC-embedding).

lower patch is fed by aperture coupling while the upper patch is coupled capacitively with the lower patch and added to increase the bandwidth of the antenna. Methods to increase patch-antenna bandwidth are:

- Increase the separation distance between the patch and the ground plane
- Incorporate slots
- Utilize lower dielectric-constant (Dk) and lower-loss (Df) materials

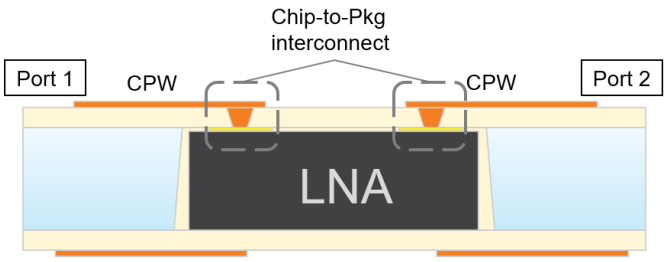

Figure 4.21: Cross-section image of an GaAs-based LNA embedded into the glass cavity.

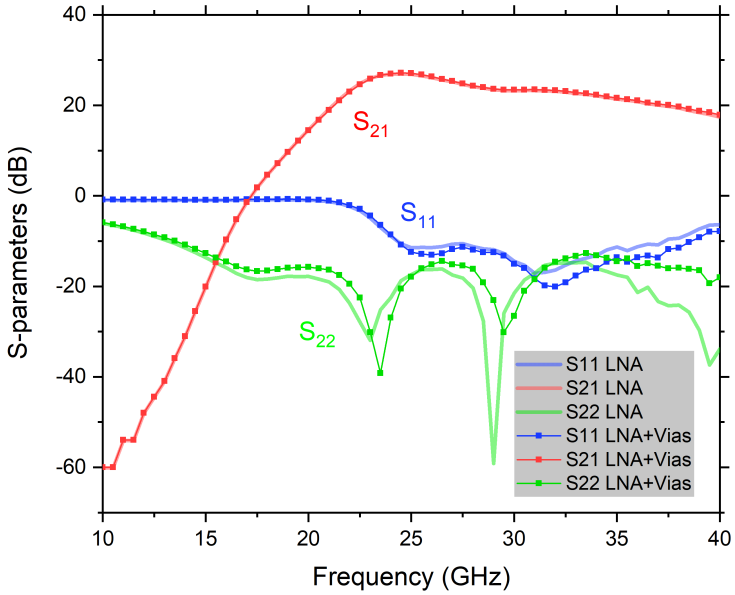

Figure 4.22: Comparison of S-parameters with and without the 80-μm microvia interconnections and CPW.

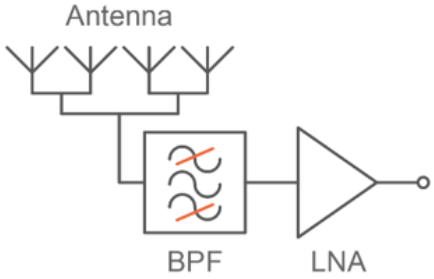

Figure 4.23: Front-end module for GPE-AiP.

- Add parasitic patch for another resonance.

Because of the antenna physics of electromagnetic radiation, antenna design is a trade-off between the antenna bandwidth enhancement and module thickness reduction. This trade-off is of significance for designers of antenna-integrated packages. As shown in [21, 27], thick substrates with more than 500-μm separation between the driven element and ground plane are preferred to cover the 28-GHz frequency bands used for 5G mobile communications. The use of low-Dk and low-Df dielectric materials, so-called low-loss materials, is also critical since these materials offer higher radiation efficiency and lower heat

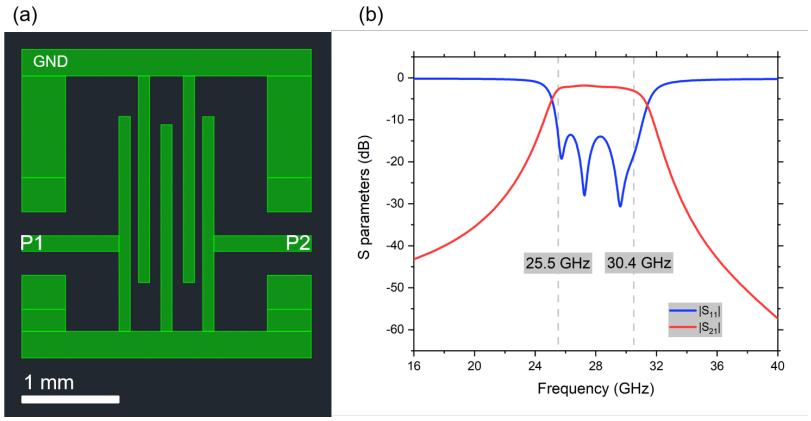

Figure 4.24: Integrated 5th-order bandpass filter covering the n257 band (a) layout and (b) S-parameters.

generation. However, high-Dk materials are needed to miniaturize the antenna as the size of patch antenna is almost $\lambda/2$, which is half wavelength on the dielectric. High Dk (Dk $>$ 5) materials can shrink the patch size and therefore mitigate the coupling with adjacent antennas that are separated with $\lambda_0/2$ (half wavelength in the air) when antenna topology is based on broad-side array. Notable disadvantages of high-Dk materials are the limited bandwidth and lower radiation efficiency because of the higher dielectric loss.

Figure 4.25 shows the antenna bandwidth obtained from the GPE-AiP stack up, indicating a nearly-linear correlation between the bandwidth and the separation distance of radiating and parasitic patches. When designing antennas, the first step is to check the return loss at the interface between the air ($Z_0 = 377\ \Omega$) and front-end module (e.g., $Z_{\text{FE}} = 50\ \Omega$ or $75\ \Omega$). S_{11}-based 10-dB and 3-dB bandwidths are widely used to quantify the bandwidth from the impedance-matching standpoint. Another key design parameter in determining bandwidths is the realized gain of the antenna, which is usually discussed in the unit of dBi. From Figure 4.25, we can see that 3-dBi-based bandwidths are approximately 1.8-GHz wider than those of S_{11}-based 10-dB bandwidths. This difference results from the dielectric and conductor losses; the dielectric loss is more predominant in the mm-wave frequency ranges. The required dielectric thickness is above 100 μm. In the stack up depicted in Figure 4.25, the low-loss dry-film dielectric provided by Taiyo Ink.

with Dk/$\text{Df}_{\text{dryfilm}}$ of 3.3/0.0025 up to 60 GHz is utilized. The use of low-loss dielectric material enables higher radiation efficiency of the antenna and higher realized-gain-based bandwidth. In contrast, the use of traditional high-Df materials results in lower realized gain and a limited gain-based bandwidth even if the S_{11}-based bandwidth covers the target frequency range of interest.

Figure 4.26 is a contour plot illustrating the impact of dissipation factor of the dielectric materials (i.e., the core and the build-up shown in the stack-up) on the realized gain of the patch antenna. Traditional materials for packaging and PCB such as FR4 offer 1.3-dBi lower realized gain per antenna element than our stack up with the lower-loss materials, with dissipation factors of $\text{Df}_{\text{glass}} = 0.0003$ and $\text{Df}_{\text{dryfilm}} = 0.0025$. Typical low-loss dielectric materials for mm-wave applications are low-loss BT resin from Mitsubishi Gas Chemical Company and Megtron-7 series from Panasonic with a Df range from 0.003 – 0.005 at 30 GHz. Such PCB-like low-loss materials could lower the process cost and are becoming popular as the manufactures supply them without enormous investment in new manufacturing just for 5G applications. One of the challenges of such PCB-like low-loss materials, however, is the difficulty of forming small features ($< \ 20\ \mu$m) . This challenge is not critical at the early stages of the 5G communication technology, but becomes more and more important when heterogeneously-integrated 5G modules are needed in the near future. The requirement of tight integration of a great number of components into 5G modules leads to the significance of package-level high-density interconnects.

Based on the studies on antenna bandwidth and realized gain along with material properties, the design and stack up of the package are determined as shown in Figure 4.27. The antenna bandwidth is enhanced with the above-mentioned techniques; dumbbell-shaped apertures in M3 increase the coupling between the feed aperture and the patches enabling good impedance matching with relatively small aperture opening and allowing dual-polarized operation [123, 124].

The return loss in Figure 4.29 shows the two nulls (resonances) induced by two patches.

The S_{11}-based 10-dB bandwidth is 25.6 GHz – 28.2 GHz (2.6 GHz), which partially covers the n257 band. In contrast, the realized-gain based 3-dBi bandwidth is 24.4 GHz – 28.6 GHz (4.2 GHz) is achieved due to the use of low-loss dielectric materials. The radiation pattern of the E-plane at 26.5 GHz is also shown in Figure 4.28. Antenna in packages for mobile applications requires a wide angle of coverage with a certain level of realized gain (˜3 dBi/element), to enable good communication between user equipment (UE) and base stations (BS) or micro/macrocell BS. These requirements come from the limited space and mobility of the handset devices. In contrast, BS or micro/macrocell BS may incorporate a larger array (8×8 or 16×16) with a higher number of channels to communicate with more UE, where the antenna gain is 1.5 – 3 dBi/element, but the total gain is increased by 35 dB [12] with combined 64 elements and a narrow beam.

4.2.3 Summary

Chip-embedded mm-wave antenna-integrated modules were demonstrated for the first time with panel-scalable 100-μm thin glass substrates in the n257 band (26.5 – 29.5 GHz). Co-design and process-development to package amplifiers, filters and antennas with minimal package parasitics is the key to realize mm-wave package systems. The first focus in this researchwas the process development towards reduced chip-to-package losses enabled by the chip-first technique into glass substrates, which led to lower signal loss than the traditional flip-chip embedding technology. The implementation of filters and integrated dual-polarized antennas was also shown. The integration challenges and trade-offs in mm-wave packages are also discussed. Overall, glass-based MMIC-embedded antenna-integrated packages are benchmarked against existing 5G substrate technologies such as organic laminate substrates and fan-out wafer level packaging.

Table 4.4: Comparison between this work and previous related work.

Work	Substrate	Frequency (GHz)	FBW (%)	Gain (dBi)	Size (λ_0)	Thickness (λ_0)	Pattern	Antenna
[115]	PCB	27.1 – 29.75	9.3	5.7	0.45 × 0.45	0.045	Azimuth	Yagi-Uda
[116]	PCB	24.5 – 31.72	25.7	4.5	0.82 × 1.98	0.056	Azimuth	SIW dipole
[117]	LTCC	26.3 – 29.79	12.4	3.1	0.18 × 0.18	0.090	Elevation	Patch
[30]	Multi-layer organic	30 – 30.8	2.6	4.9	0.6 × 0.6	0.082	Elevation	Patch
[53]	Glass	47.2 – 67	33	3.5	0.82 × 1.00	0.060	Azimuth	Taper-slot
This work	Glass with build-up	21.9 – 29.8	28.2	4.8	0.34 × 0.40	0.028	Azimuth	Yagi-Uda

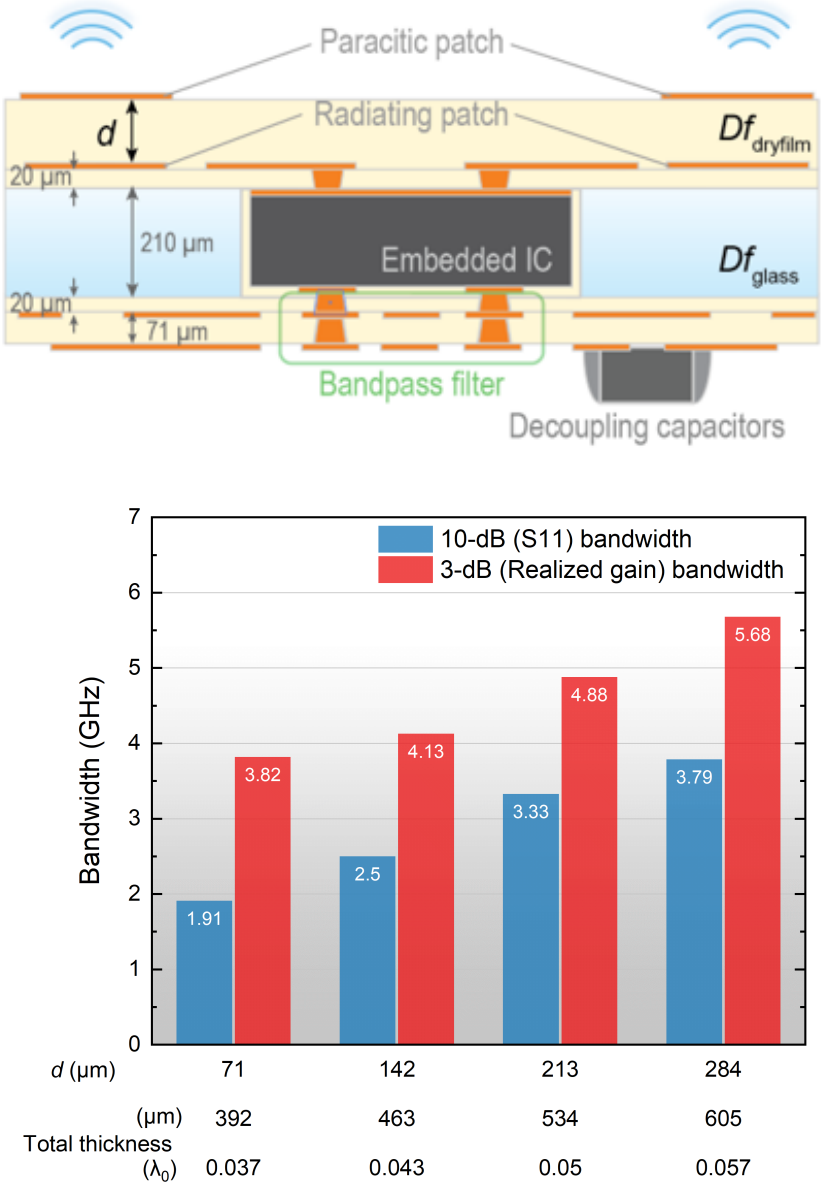

Figure 4.25: Top: Stack-up of GPE-AiP for the study of packaging structures and materials with the impact on antenna performance. Bottom: Bandwidth dependence on the dielectric thickness, d.

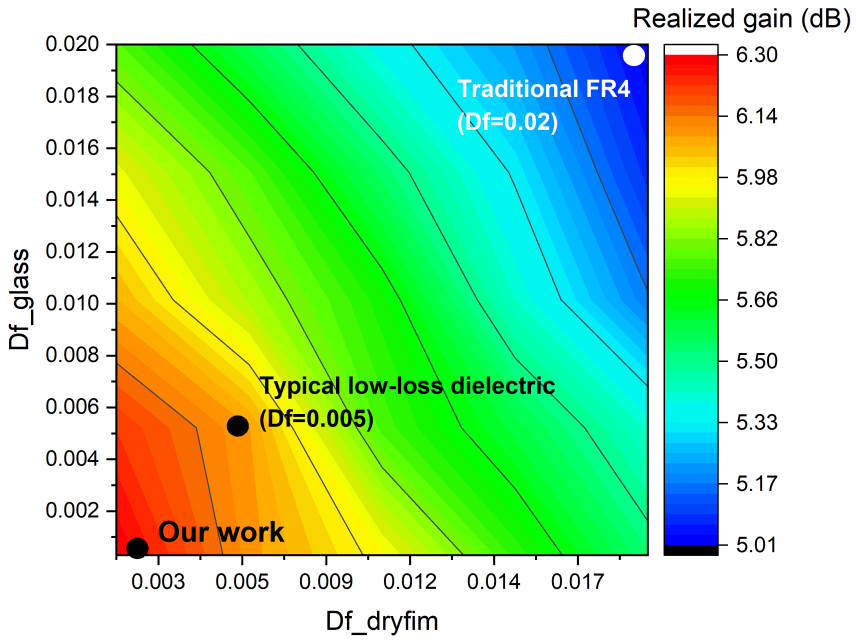

Figure 4.26: The impact of dissipation factor, Df, on the realized gain of antenna.

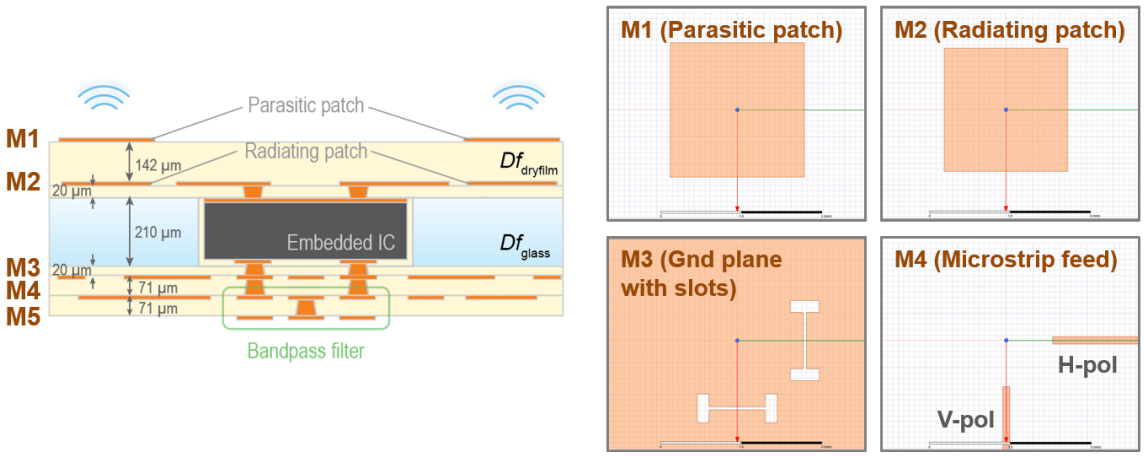

Figure 4.27: Cross-section image of aperture-coupled stacked-patch antennas and integrated bandpass filters with the detailed top views of the antenna.

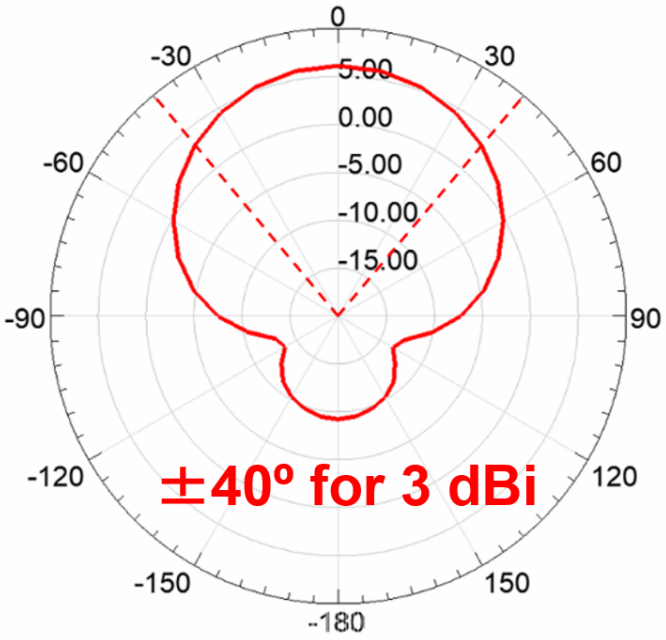

Figure 4.28: Radiation pattern of the E-plane at 26.5 GHz covering $\pm 40°$.

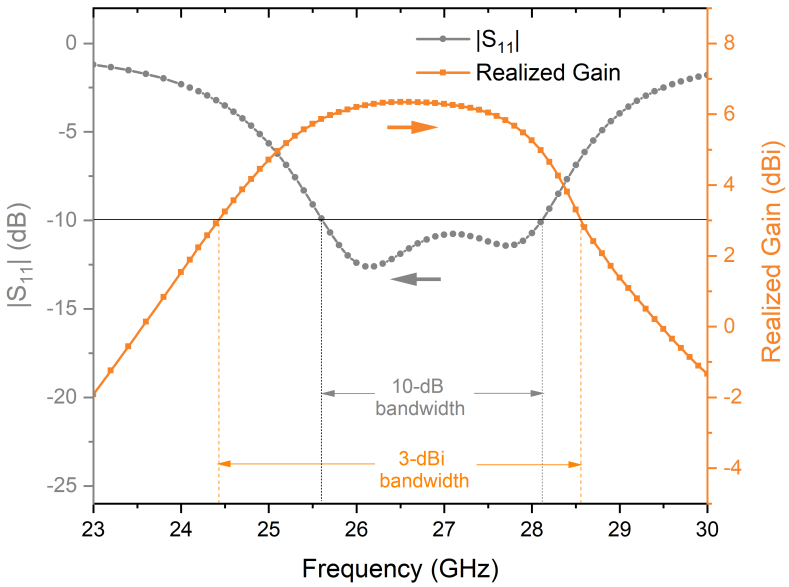

Figure 4.29: Frequency responses of the stacked-patch antenna with the return loss and realized gain.

CHAPTER 5
RESEARCH SUMMARY, NOVELTY WITH CONTRIBUTIONS, AND SUGGESTIONS FOR FUTURE WORK

The objective of this dissertation is to model, design, and demonstrate high-performance, and ultra-thin antenna-integrated 3D glass-based mm-wave packages. Glass-based 5G mm-wave antenna module integration was proposed to achieve superior performance with miniaturization and manufacturability. The package-level integration of mm-wave devices and components into glass substrates offer higher component density, lower component-to-component signal losses, smaller footprint, and thickness reduction compared to conventional organic- or ceramic-based substrates because of:

- Superior dimensional stability
- Availability in large-area low-cost panels
- Ability to form fine-pitch through-vias
- Stability to temperature and humidity
- Matched CTE with devices
- Tailorable dielectric constants and loss tangent
- Transparency of the substrate.

Taking advantage of these properties of glass substrates, research and development of glass substrates for RF applications have been performed with the 3D IPAC approach [125] and panel-level glass IPD interposer [41] in the past decade. However, despite the superior glass properties, integrated mm-wave 3D glass packages have not been reported.

The research specifically exploits the beneficial glass properties that make them ideal for superior system performance in the mm-wave frequency range (>20 GHz). In order to design and demonstrate high-performance, and ultra-thin antenna-integrated 3D glass-based mm-wave packages, key building blocks that are critical in antenna-integrated modules are identified as follows: 1) low-loss interconnects between components that are integrated into a mm-wave module; and 2) constrained physical dimensions that limit the design flexibility and miniaturization. To address these technical challenges, electrical modeling of 5G antenna-integrated mm-wave modules, 3D glass mm-wave package fabrication with process development to achieve geometry control and high-precision copper patterning are performed to achieve the performance metrics.

Details of the electrical modeling, design, fabrication, and assembly processes as well as results and analyses for both building blocks and antenna-integrated modules were presented in the previous chapters. The proposed glass-substrate-based antenna-integrated modules were validated through model-to-hardware correlations along with comparison to state-of-the-art research. Key research findings associated with research tasks are compiled in the first section of this chapter. This is then followed by a summary of key contributions of this research and a discussion on the potential research opportunities. The last part of this chapter lists publications and awards from this research.

5.1 Research Summary

5.1.1 Low-Loss High-Density Package-Level Interconnects

Precisely-fabricated impedance-matched interfaces, low-loss interconnections, and feed-lines play significant roles in enabling the high performance of antennas and distributed passives in 5G packages. The first part of this dissertation focused on the design, fabrication and demonstration of low-loss signal routing for 5G systems. The three research tasks for this part are summarized in Figure 5.1.

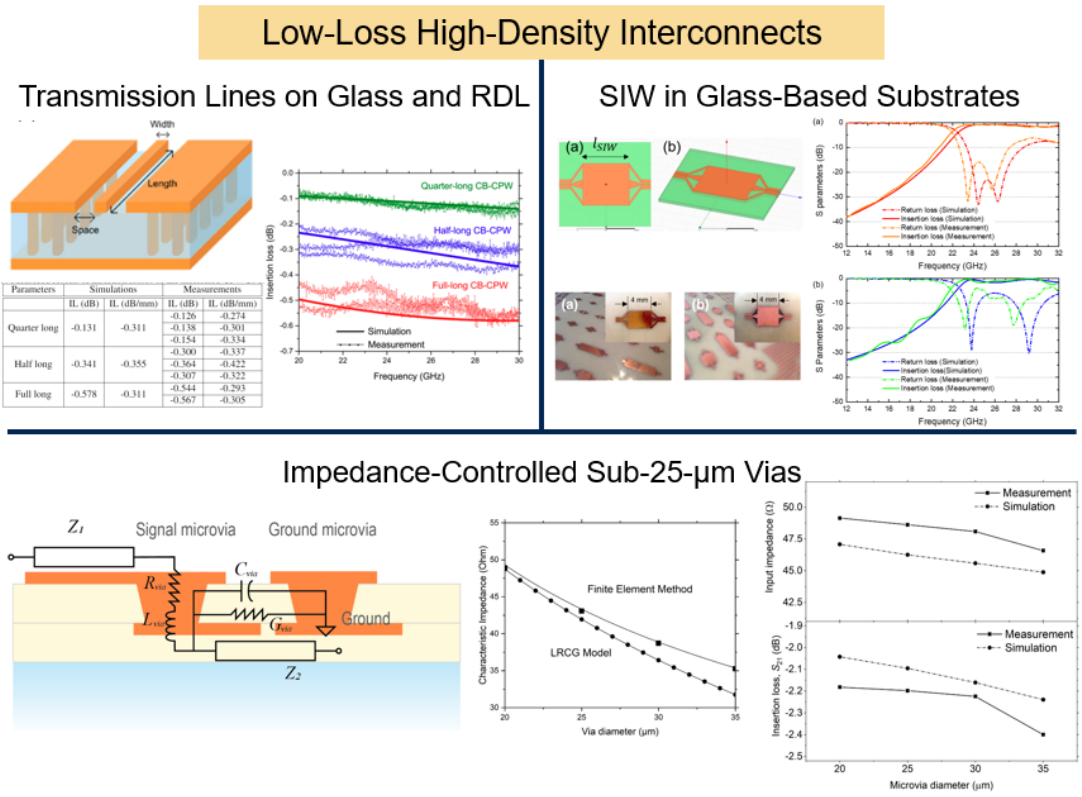

Figure 5.1: Research tasks for low-loss high-density package-level interconnects.

Transmission Lines on Glass and Redistribution Layers

To show the initial electrical performance of glass-based packaging substrates, conductor-backed coplanar waveguide patterned on the stack-up of a 130-μm glass core laminated with 30-μm ABF GY-11 was studied in the frequency band of 20 – 30 GHz. The stack up consists of a metal layer on each side of the glass substrate, where the ground plane atop the glass substrate is electrically connected to the bottom ground plane through-glass vias. Various lengths of GB-CPW were fabricated through semi-additive patterning (SAP) process, along with the inspection of geometries of fabricated structures. Relatively good model-to-hardware correlation was obtained from the high-frequency measurements for 0.42-mm, 0.9-mm, and 1.86-mm CB-CPWs with measured insertion losses of 0.2 – 0.3 dB/mm at 28 GHz. This relatively-high insertion loss results from the comparatively-high loss tangent ($\tan\delta$=0.007).

The second part of the chapter discussed high-precision low-loss signal routing in redistribution layers. Various topologies of transmission lines and interconnects were modeled and designed low-loss dielectric thin-films. The simulated results for insertion losses of transmission lines (i.e., microstrip lines and striplines) and microvia transitions were correlated with the measured values on glass substrates with low-loss dielectric thin-films. Transmission lines in RDLs showed an averaged insertion loss of 0.103 dB/mm, while that of microvia was observed to be 0.038 dB/microvia. Along with the reduction in the overall package foot-print, about 3X reduction in link-budget losses compared to fanout wafer level packaging is shown to be feasible with the proposed 3D glass packages.

Future work — For next-generation highly-integrated 5G/6G modules, efforts to mitigate signal losses and control impedance in multi-layered fine-feature RDLs should be made. In such high-density package-level signal routing (line width $< \ 20\ \mu$m), control of surface roughness and dielectric thickness ($< \ 30\ \mu$m) is extremely critical to obtain the desired performance of integrated components such as antenna array, passive elements, and beam-forming or power-management ICs. Minimizing the conductor loss becomes more significant than reducing the dielectric loss in such high-density RF packages.

Substrate-Integrated Waveguides in Glass-Based Substrates

Innovative low-loss glass substrates with fused silica are studied as a replacement to traditional glass substrates for packaging. The section began with characterization of the dielectric constants of the novel silica substrate. The characterization results show ultra-low dissipation factors ($\tan\delta$) around 28 GHz. This section also discussed the demonstration of substrate-integrated waveguides for the 28-GHz band with borosilicate glass and fused silica, and compared them with other leading-edge low-loss organic-based substrates. The de-embedded insertion loss based on TRL calibrations showed 0.018 dB/mm. The SIWs using borosilicate glass or fused silica can be extended to other applications such as low-pass or

bandpass filters and low-foot print package-integrated antennas. The research demonstration highlights the potential of glass-based substrates as a thin core substrate for mm-wave applications.

Future work — One of the notable challenges of SIW is the bulky size, which is nearly proportional to the wavelength. The glass-based SIWs investigated in this dissertation are designed for the 28-GHz bands and larger than $4 \times 3\,\text{mm}^2$. This feature of SIW, however, leads to the high potential in higher frequency ranges such as W or D bands (70 – 170 GHz), where the size could be 3X smaller than that at 28 GHz. SIWs in the W and D bands can be extended to band-selection filters, antennas, and other passive components.

Impedance-Controlled Sub-25-Micron Vias

Low-loss small microvias are demonstrated in build-up layers for the next-generation heterogeneous high-density high-performance 5G mm-wave packages. In order to minimize the signal losses and identify the required microvia diameters, an equivalent circuit was modeled and quantified with LRCG and FEM methodologies. Based on the models and simulated characteristic impedance, test vehicles with daisy chains were fabricated in build-up layers on a core package substrate. The daisy chains included microstrip lines and striplines as in-plane signal routing and microvias as vertical connections with various microvia diameters. The high-frequency measurements were performed to verify the models and simulated results in the 28 GHz band. The characterization results exhibited good model-to-hardware correlation and indicate that small microvias (20 μm) provides impedance closer to 50 Ω compared to the microvias larger than 35 μm. This matched microvia impedance have led to low reflection and insertion loss, resulting in 10% reduction in signal losses caused by microvias in the 5G New-Radio n257 band around 28 GHz. The detailed study on low-loss microvias indicated that not only do small microvias offer the potential towards high-density signal routing, but they also provide low insertion losses as they lead to highly impedance-matched systems.

Future work — Sub-25-μm vias become imperative when heterogeneously-integrated RF/mm-wave packages are needed. Small microvias or blind vias not only provide higher density of signal/power distribution, but also enable impedance control of the channels in the packages as discussed in this dissertation. Further research on surface roughness and staggered vias along with through package vias and landing pads for BGAs, C4 bumps, copper-pillar assembly will be an important topic for more compact and higher performance wireless electronics.

5.1.2 Design and Demonstration of Glass-Based Antenna-Integrated mm-wave Modules

This chapter discussed the design and demonstration of antenna-integrated glass-based packages for 28-GHz bands. The first packaging architecture is the *chip-last* or flip-chip antenna module, focusing on package-level design for antenna-integration and package miniaturization, process development for low-loss interconnects with through glass vias, and the characterization of key building blocks: 1) co-planar waveguides and TPVs, 2) dipole Yagi-Uda antenna, and 3) flip-chip assembled LNA with 80-μm solder balls. The second packaging architecture is the *chip-first* or glass-panel embedding (GPE) approach for antenna integration. This part also discussed the process development, followed by the integration of band-selection filters and dual-polarized patch antenna array while quantifying the benefits of the GPE architecture for AiP applications. The research tasks for this part are summarized in Figure 5.2.

Ultra-Thin Antenna-Integrated Glass-Based mm-Wave Package

This section presented heterogeneous integration of antenna-in-package, seamless or low-loss antenna-to-receiver signal transitions, and flip-chip assembly on panel-scale ultra-thin glass substrates, in the 28 GHz band for high-speed 5G communication standards. The key benefits of glass core such as dimensional stability, thickness control, unique laminated glass stack-up, and via-in-via processes result in process stability and design flexibility for

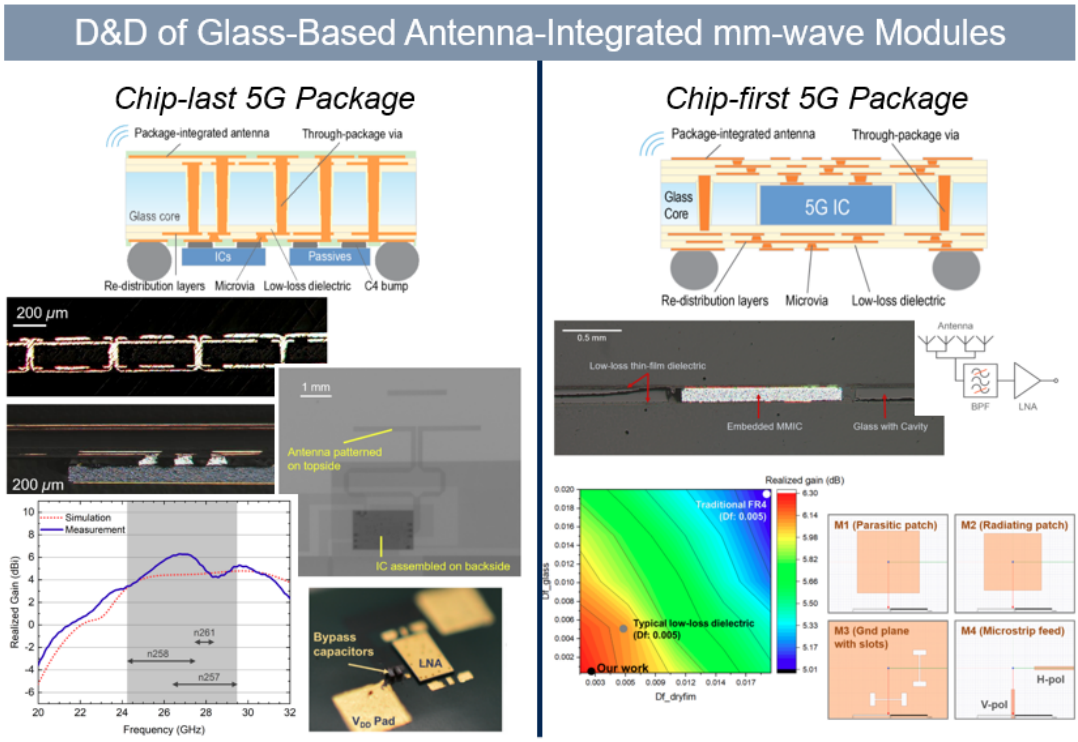

Figure 5.2: Research tasks for the design and demonstration of glass-based antenna-integrated mm-wave packages.

system design. Module-level characterization results highlight the low interconnect signal losses with a through-package-via loss of 0.021 dB/TPV at 28 GHz. The Yagi-Uda antenna fabricated on glass substrates showed a center frequency of 25.85 GHz with a fractional bandwidth of 28.2%, which covers the 28GHz 5G frequency bands of interest. The antenna also featured a wide-angle main lobe at the target frequency range, implying good coverage of signal transmission and reception. Overall, this research reports package-integrated antenna, feedlines, low-loss interconnects, and assembly of active ICs and discrete passive components implemented with 100-μm glass-substrate technology.

Future work — mm-wave packages entail co-design and integration of phased antenna array with transceiver or beamforming ICs to meet the power distribution and signal integrity requirements, and passive components to support all the functions with minimal parasitics and interference. The co-design of packages from the electrical, thermal, and mechanical standpoints is critical to ensure performance, manufacturing and reliability. Glass-based

module-level research or demonstration with thermal management has yet to be reported. Thermal management of mm-wave modules will be critical in high-power applications such as macrocells and basestations, and need to be addressed with innovative approaches.

Glass-Based IC-Embedded Antenna-Integrated mm-wave Packages

A chip-embedded mm-wave antenna-integrated module was demonstrated for the first time with panel-scale 100-μm glass substrates in the n257 band (26.5 – 29.5 GHz). Co-packaging of amplifiers, filters and antennas with minimal package parasitics is the key to realize mm-wave package systems. The first focus was the process development towards reduced chip-to-package losses enabled by the chip-fist technique into a glass substrate, which led to lower signal loss than the flip-chip embedding technology. The implementation of filters and integrated dual-polarized antennas was also shown. The integration challenges and trade-offs in mm-wave packages are also discussed. Overall, glass-based MMIC-embedded antenna-integrated packages are benchmarked with existing 5G substrate technologies such as organic laminate substrates and fan-out wafer level packaging.

Future work — Embedding or fan-out technology has become one of the key packaging structures for heterogeneous integration especially for high-performance computing. This trend can be seen recently in RF/mm-wave packages as well. Although this dissertation focused on the 28-GHz frequency band for 5G communication networks, ultra-thin GPE-AiP should be beneficial in higher frequency ranges (> 60 GHz) because the implementation of patch antennas requires higher electrical length between the patch and ground plane for enhanced bandwidth. GPE-AiP with a total thickness less than 400 μm is slightly too thin to cover wide-enough frequency bands (24.25 – 29.5 GHz and 37 – 40 GHz), and therefore can be an excellent candidate for mm-wave packages in the V (40 – 75 GHz), W, and D bands. In addition, thermal management is one of the most critical challenges in IC-embedded packages, which must be addressed as well.

5.2 Novelty of Research

The novelty of the research discussed in this dissertation is summarized in the following categories: 1) Design of antenna-integrated glass-based packages, 2) Fabrication of 5G antenna-integrated modules with high-density interconnects, 3) Comprehensive Characterization of fabricated test vehicles from fabrication, 5G performance, and reliability stand-points, and 4) Industrial impact.

Design of glass-based antenna-integrated packages

Glass-based antenna-integrated packages were designed for the first time with a 100-μm glass with build-up layers. Fundamental design research on transmission lines, SIWs, and microvias were also performed addressing the mm-wave specific challenges in fabrication and measurements. Inter-disciplinarity enabled the first demonstration of 5G glass-based antenna-integrated package, and its miniaturization.

Fabrication of 5G antenna-integrated modules with high-density interconnects

Designed test vehicles were fabricated by the author in conjunction with PRC members. The fabrication starts from a bare glass, experiences all semi-additive processes, and assembly in D&D modules. Fabrication of 3D packages with precise metal patterning is more critical in mm-wave frequency ranges than in the sub-6 GHz frequency bands. Optimized fabrication processes with 1-μm precision were developed to provide good hardware-to-mdel correlation and stable electrical performance in 6-inch panels. The design rules and guidelines are also completed based on the process feasibility and fabrication experience.

Comprehensive Characterization of fabricated test vehicles from fabrication, 5G performance, and reliability stand-points

Fabricated test vehicles were characterized from electrical, mechanical, chemical and ma-

terials stand-point. In addition to high-frequency measurements based off vector network analyzers, surface roughness, mechanical warpage due to the unbalanced metal density on either side of the packaging substrate, and adhesion strength of copper onto dielectric layers were found to impact the fabrication, performance and reliability. These non-electrical characterization techniques also assist mm-wave package designers to anticipate model-to-hardware discrepancies, identify root causes, and incorporate design revisions in subsequent iterations, which is one of the notable strengths of interdisciplinary research. The work presented in this dissertation included electrical characterizations, along with package-level interdisciplinary designs and process development.

Industrial impact

This research on the design and development of glass-based antenna-integrated mm-wave packages has provided scientific and engineering foundation and addressed key technical barriers to prepare industry supply-chain and end-users for 3D glass substrate manufacturing by involving the following companies: Qualcomm, Samsung, Qorvo, Northrop Grumman Corporation, AGC, Corning, Schott, Hitachi Metals, NGK-NTK, Murata, Nagase, JSR, Ajinomoto, Taiyo Ink., Tango Systems, Atotech, Analog Devices, Panasonic, and other leading-edge companies.

5.3 Suggestions for Future Work

Extension to 6G Application

Many of the traditional approaches used for RF packages are not applicable to sub-THz and THz radios [126]. Sub-THz or 6G communications focus on heterogeneous package integration, as illustrated in Fig. 5.3 by incrementally advancing the system components such as precision antenna arrays, low-loss interconnects and waveguides and active devices. As frequency increases into the THz region, we will not be able to employ the techniques used for low frequencies because of multiple challenges associated with signal loss, need

for nano-scale III-V front-end devices in close proximity with CMOS beamforming chips, and antenna arrays and interconnects with advanced materials. The current interconnection techniques such as wire bonding or solder-based bumps are too bulky; therefore, excitation of multimode, radiation, and reflection would adversely affect the electrical performance. As the skin depth is approximately 120 nm at 300 GHz, higher frequency packaging will require shorter interconnects and smooth surface to mitigate conductor loss. Radiation loss must be minimized as well with good impedance matching and high-precision manufacturing with tolerance below 1 μm. Dielectric loss is more predominant in sub-THz or THz bands, which translates to the need for accurate characterization of potential materials at those high frequencies. Another key metric in THz applications is antenna implementation. While AiP approach is viable, antennas or radiators on ICs will play a significant role. THz antenna arrays (e.g., 1024 elements in 1 mm^2) will be integrated with graphene-based radiation sources and detectors, lenses, and intelligent metasurfaces with space-time-frequency coding and low-loss interconnects.

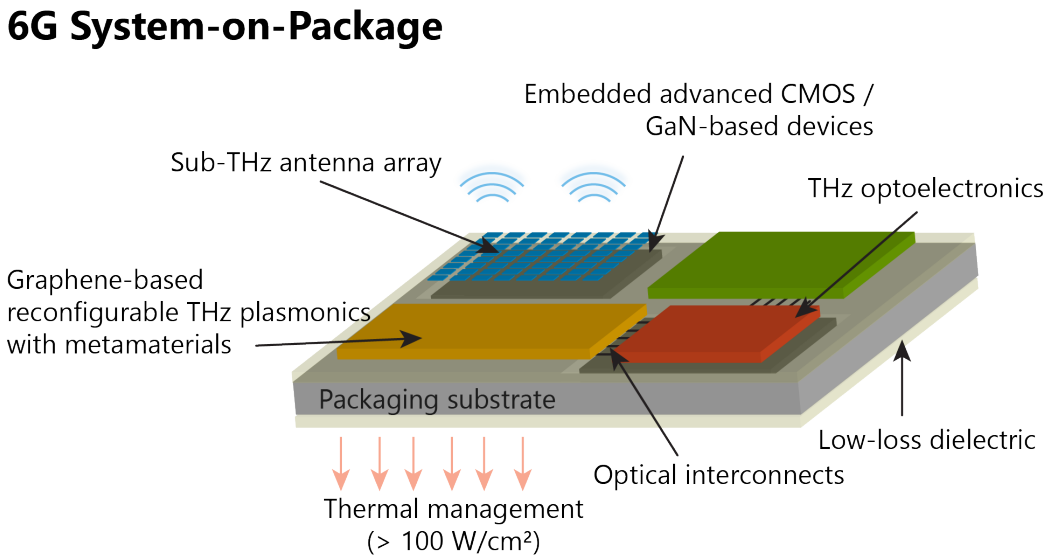

Figure 5.3: Conceptual diagram of heterogeneously-integrated quasi-optical THz package for 6G communications.

Figure 5.3 shows a conceptual diagram of heterogeneously-integrated quasi-optical

THz 6G package for a device with an antenna, where sub-THz or THz waves will be radiated into the air from reconfigurable AiP or the on-chip antenna [127]. Along with the 3D integration of CMOS with III-V nanodevices, ultra-wide band low-loss interconnections and integration of precision antenna arrays with filters and power-dividing networks, technical challenges such as heat management and EMI shielding must be also addressed for such high-frequency systems.

5.4 Publications and Awards

The research outcomes from this dissertation and other related research activities have resulted in the following peer-reviewed journal papers, conference proceedings, and awards.

Peer-Reviewed Journals

1. A. O. Watanabe *et al.*, "Ultrathin Antenna-Integrated Glass-Based Millimeter-Wave Package With Through-Glass Vias," in *IEEE Transactions on Microwave Theory and Techniques*, doi: 10.1109/TMTT.2020.3022357 [87].

2. A. O. Watanabe, B. K. Tehrani, T. Ogawa, P. M. Raj, M. M. Tentzeris and R. R. Tummala, "Ultra-low-Loss Substrate-Integrated Waveguides in Glass-Based Substrates for Millimeter-Wave Applications," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 3, pp. 531-533, March 2020, doi: 10.1109/TCPMT.2020.2968305 [128].

3. A. O. Watanabe, H. Ito, R. P. Markondeya, R. R. Tummala and M. Swaminathan, "Low-Loss Impedance-Matched Sub-25-μm Vias in 3-D Millimeter-Wave Packages," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, no. 5, pp. 870-877, May 2020, doi: 10.1109/TCPMT.2020.2982294 [45].

4. A. O. Watanabe, P. M. Raj, D. Wong, R. Mullapudi, and R. Tummala, "Multilayered Electromagnetic Interference Shielding Structures for Suppressing Magnetic Field Coupling," *Journal of Electronic Materials*, vol. 47, no. 9, pp. 5243–5250, 2018, doi: 10.1007/s11664-018-6387-2 [129].

5. A. O. Watanabe, M. Ali, S. Y. B. Sayeed, Rao Tummala, and P. M. Raj, "A Review of 5G Systems Package Integration," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, accepted for publication [130].

6. M. Ali, F. Liu, A. Watanabe *et al.*, "First Demonstration of Compact, Ultra-Thin Low-Pass and Bandpass Filters for 5G Small-Cell Applications," in *IEEE Microwave*

and Wireless Components Letters, vol. 28, no. 12, pp. 1110-1112, Dec. 2018, doi: 10.1109/LMWC.2018.2876769 [113].

7. M. Ali, A. Watanabe, T. Lin, D. Okamoto, P. M. Raj, M. Tentzeris, and R. Tummala, "Package-Integrated, Wideband Power Dividing Networks and Antenna Arrays for 28 GHz 5G New Radio Bands," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, accepted for publication.

8. M. Ali, A. Watanabe, T. Kakutani, P. M. Raj, R. Tummala, and M. Swaminathan, "Package Integration and System Performance Analysis of Glass-based Passive Components for 5G New Radio Millimeter-Wave Modules," in *IEEE Transactions on Microwave Theory and Techniques*, under review.

9. F. Liu, G. Khurana, R. Zhang, A. Watanabe, B. DeProspo, C. Nair, R. Tummala, and M. Swaminathan., "Innovative Sub-5-μm Microvias by Picosecond UV Laser for Post-Moore Packaging Interconnects," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 10, pp. 2016-2023, Oct. 2019, doi: 10.1109/TCPMT.2019.2941866 [106].

10. Y. Wang, A. O. Watanabe, N. Ogura, P. M. Raj, and R. Tummala, "Sintered Nanocopper Paste for High-Performance 3D Heterogeneous Package Integration," *Journal of Electronic Materials*, vol. 49, no. 11, pp. 6737–6745, 2020 [131].

Conference Proceedings

1. A. O. Watanabe *et al.*, "Glass-Based IC-Embedded Antenna-Integrated Packages for 28-GHz High-Speed Data Communications," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, accepted.

2. A. O. Watanabe *et al.*, "Low-Loss Additively-Deposited Ultra-Short Copper-Paste Interconnections in 3D Antenna-Integrated Packages for 5G and IoT Applications," *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 972-976, doi: 10.1109/ECTC.2019.00152.

3. A. O. Watanabe *et al.*, "Design and demonstration of ultra-thin 3D glass-based 5G modules with low-loss interconnects," *2018 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)*, Mie, 2018, pp. 180-183, doi: 10.23919/ICEP.2018.8374698.

4. A. Watanabe *et al.*, "Leading-Edge and Ultra-Thin 3D Glass-Polymer 5G Modules with Seamless Antenna-to-Transceiver Signal Transmissions," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, 2018, pp. 2026-2031, doi: 10.1109/ECTC.2018.00304.

5. A. O. Watanabe *et al.*, "First Demonstration of 28 GHz and 39 GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules," *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 236-241, doi: 10.1109/ECTC.2017.329.

6. A. O. Watanabe *et al.*, "Highly-Effective Integrated EMI Shields with Graphene and Nanomagnetic Multilayered Composites," *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, 2016, pp. 206-210, doi: 10.1109/ECTC.2016.294.

7. M. Ali, A. Watanabe, T. Kakutani, P. M. Raj, R. Tummala, and M. Swaminathan, "Heterogeneous Integration of 5G and Millimeter-Wave Diplexers with 3D Glass Substrates," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, accepted.

8. T. Kakutani, M. Ali, A. Watanabe *et al.*, "Heterogeneous Integration of 5G and Millimeter-Wave Diplexers with 3D Glass Substrates," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, accepted.

9. P. Nimbalkar, F, Liu, A. Watanabe *et al.*, "Fabrication and Reliability Demonstration of 5µm Redistribution Layer Using Low-Stress Dielectric Dry Film," *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, accepted.

10. M. Ali, A. Watanabe, T. Lin, M. R. Pulugurtha, M. M. Tentzeris and R. R. Tummala, "3D Glass Package-Integrated, High-Performance Power Dividing Networks for 5G Broadband Antennas," *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 960-967, doi: 10.1109/ECTC.2019.00150.

11. T. Sun, R. G. Spurney, A. Watanabe, *et al.*, "3D Packaging with Embedded High-Power-Density Passives for Integrated Voltage Regulators," *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 1300-1305, doi: 10.1109/ECTC.2019.00201.

12. H. Ito, K. Kanno, A. Watanabe *et al.*, "Advanced Low-Loss and High-Density Photosensitive Dielectric Material for RF/Millimeter-Wave Applications," *2019 International Wafer Level Packaging Conference (IWLPC)*, San Jose, CA, USA, 2019, pp. 1-6, doi: 10.23919/IWLPC.2019.8914136.

13. G. Park *et al.*, "Design and Measurement of a 28 GHz Glass Band Pass Filter based on Glass Interposers for 5G Applications," *2019 Electrical Design of Advanced Packaging and Systems (EDAPS)*, KAOHSIUNG, Taiwan, 2019, pp. 1-3, doi: 10.1109/EDAPS47854.2019.9011679.

14. N. Ogura, S. Ravichandran, T. Shi, A. Watanabe, S. Yamada, M. Kathaperumal, and R. Tummala, "First demonstration of ultra-thinglass panel embedded (GPE) package with sheet type epoxy molding compound for 5G/mm-wave applications," in *International Symposiumon Microelectronics*, vol. 2019, no. 1. International Microelectronics Assembly and Packaging Society, 2019, pp. 000 202–7.

15. F. Liu, C. Nair, G. Khurana, A. Watanabe *et al.*, "Next Generation of 2-7 Micron Ultra-Small Microvias for 2.5D Panel Redistribution Layer by Using Laser and Photolithography Technologies," *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2019, pp. 924-930, doi: 10.1109/ECTC.2019.00144.

16. M. Ali, A. Watanabe, T. Lin, M. Tentzeris, R. Tummala and P. M. Raj, "Ultra-Wideband, Glass Package-Integrated Power Dividers for 5G and mm-Wave Applications," *2019 IEEE International Symposium on Antennas and Propagation and USNC-URSI Radio Science Meeting*, Atlanta, GA, USA, 2019, pp. 863-864, doi: 10.1109/APUSNCURSINRSM.2019.8888980.

17. G. Park *et al.*, "Design and Analysis of Receiver Channels of Glass Interposers for 5G Small Cell Front End Module," *2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, San Jose, CA, 2018, pp. 107-109, doi: 10.1109/EPEPS.2018.8534215.

18. M. Ali, F. Liu, A. Watanabe *et al.*, "Miniaturized High-Performance Filters for 5G Small-Cell Applications," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, 2018, pp. 1068-1075, doi: 10.1109/ECTC.2018.00164.

19. V. Sundaram *et al.*, "Integrated Copper Heat Slugs and EMI Shields in Panel Laminate (LFO) and Glass Fanout (GFO) Packages for High Power RF ICs," *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 300-305, doi: 10.1109/ECTC.2017.339.

20. T. Lin, P. M. Raj, A. Watanabe *et al.*, "Nanostructured miniaturized artificial magnetic conductors (AMC) for high-performance antennas in 5G, IoT, and smart skin applications," *2017 IEEE 17th International Conference on Nanotechnology (IEEE-NANO)*, Pittsburgh, PA, 2017, pp. 911-915, doi: 10.1109/NANO.2017.8117483.

Awards

1. IEEE Electronic Packaging Society Japan Chapter Young Award 2018.
2. Most Popular Conference Paper 2017 in IEEE Electronics Packaging Society (EPS)
3. Best Student Paper in Future Car Workshop 2016 by SEMI, IEEE, CPMT, iMAPS, iNEMI.

Review Activities

- IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT): 2019 – Present
- IEEE Transactions on Microwave Theory and Techniques (T-MTT): 2020 – Present

- ELSEVIER Applied Materials Today: 2019 – Present
- Cambridge University Press International Journal of Microwave and Wireless Technologies: 2020 – Present

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